CMT211x/5x/8x Transmitter Chip Schematic and PCB Layout Design Guide

Overview

This document provides the schematic and PCB layout design guidelines for users engaging in the development based on the transmitter chips of CMOSTEK NextGenRF™ product family. The document aims for guiding users to efficiently fulfill target performance objectives such as output power, transmitting current and spurious & harmonic suppression.

The product models covered in this document are shown in the table below.

Table 1. Product Models Covered in This Document

Product Model	Frequency (MHz)	Modulation Method	Chip Function	Configuration Method	Package
CMT2110A	240 - 480	OOK	Single-wire, direct mode, transmitter-only	EEPROM	SOT23-6
CMT2117A	240 - 960	OOK	Single-wire, direct mode, transmitter-only	EEPROM	SOT23-6
CMT2119A	240 - 960	(G)FSK/OOK	Single-wire, direct mode, transmitter-only	EEPROM/Registers	SOT23-6
CMT2150A	240 - 480	OOK	7- key transmitter with encoder	EEPROM	SOP14
CMT2157A	240 - 960	(G)FSK/OOK	7- key transmitter with encoder	EEPROM	SOP14
CMT2180A	240 - 480	OOK	Transmitter-only Soc	EEPROM	SOP14
CMT2189A	240 - 960	(G)FSK/OOK	Transmitter-only Soc	EEPROM	SOP14

This document will discuss several considerations for the usage of CMOSTEK NextGenRF™ transmitter-only series chips.

- Matching network
- Crystal circuit
- Digital signal
- Power supply and ground design
- Power optimization considerations
- Pressed-key circuit design
- Test circuit design
- Design check items

Table of Contents

1 Matching Network Design

The matching network transforms the chip output pin impedance into the antenna impedance to achieve the following design goals.

1. Maximize output power.
2. Maximize efficiency and minimize power consumption while meeting output power requirements.
3. Control harmonics and spurs to meet ETSI, FCC and other specifications.
4. Minimize material BOM, system cost, etc.

However, subject to the product structure, size, materials, etc. of a specific application, sometimes it's hard to achieve all above objectives at the same time. Thus users need to have a balance among above objectives according to requirement priority.

Taking the CMOSTEK EM board as an example, the following sections will discuss how to choose an appropriate matching network to optimize various objectives according to different application and system requirements.

1.1 Single-ended Output Matching Network Design

The general schematic of the single-ended RF output is shown in the below figure.

The matching network in the below figure can be implemented via 3 to 7-order filters according to different application requirements such as transmit power size, cost requirements, whether it needs to pass CE/FCC specification, single-ended or differential output, etc.

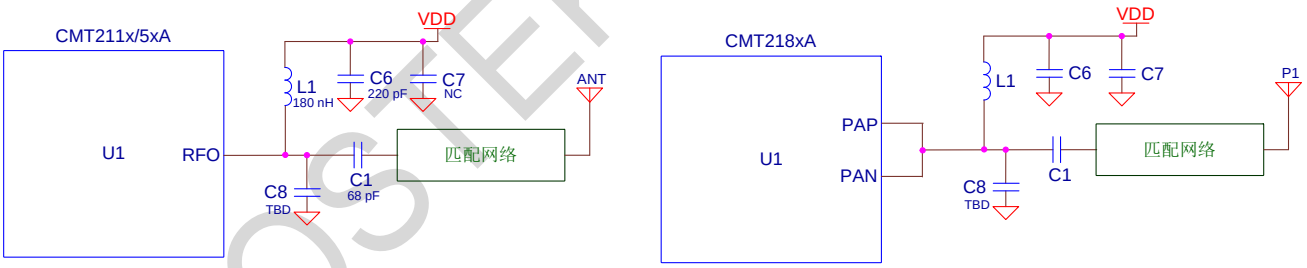

Figure 1. CMT211x/5x/8xA Single-ended Output Matching Network Design

Notes:

1. Circuit schematics other than the RF output ones are not included in the above figure.
2. L1 is the energy absorbing (chock) inductor.
3. C6 and C7 are power supply decoupling capacitors (C7 is optional) to reduce the PA output's impact on the power supply. Users should choose them according to usage environments.
4. C8 is an optional capacitor for fine-tuning the matching network. When the performance of the matching network can meet requirements, it's not necessary to solder C8.
5. C1 is a DC blocking capacitor.
6. The DEMO board provided by CMOSTEK uses a glue stick antenna, namely ANT antenna. In practical applications, users

can change it to other types of antennas such as PCB antennas, wire antennas or spring antennas according to actual needs. It should be noted that selecting different antennas will affect the selection of the matching network and various component values. Due to the wide variety of antennas, for description convenience, this document will discuss based on the example of a matching network with a 50 Ω impedance glue stick antenna.

7. The single-ended output of the CMT218xA needs to be connected to the matching network before connecting PAP/PAN.

8. Users can change the transmission power in the below 2 ways.

   a) Set the Tx Power parameter through the USB Programmer and RFPDK to change the chip transmission power.

   b) Place a resistor (not shown in the above figure) between the energizing inductor and the power supply. Users can adjust the transmitting power by changing the resistance value. The presence of this resistor will reduce the transmission efficiency. So it is recommended to change the transmission power by changing the chip's transmission power settings.

9. The purpose of matching is to match the output impedance to the network matching antenna impedance. The output impedance of the RFO pin at different frequencies is shown in the below table.

Table 2. RFO Pin Output Impedance @315/433.92/868.35/915 MHz

Frequency (MHz)	R_{INT} (Ω)	C_{INT} (pF)
315	150	6.3
433.92	120	6.8
868	90	7.2
915	80	7.4

10. PCB loop antennas (loop antennas) are often used in low-cost applications where product size is limited. A spare ground capacitance C9 is added to the end of the antenna trace to make it more flexible to debug transmission power as shown in the below figure.

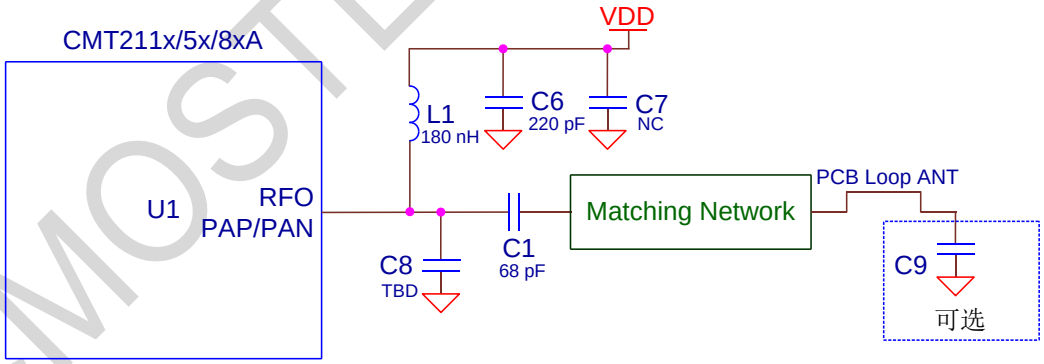

Figure 2. CMT211x/5x/8xA Single-ended Output PCB Antenna Circuit Design

1.1.1 RF Output Design Meeting ETSI/FCC/3C Certification

Standards such as ETSI/FCC/3C have strict requirements on emission and spurs. CMOSTEK recommends to apply 5 to 7-order low-pass filter networks for matching as shown in the below figure.

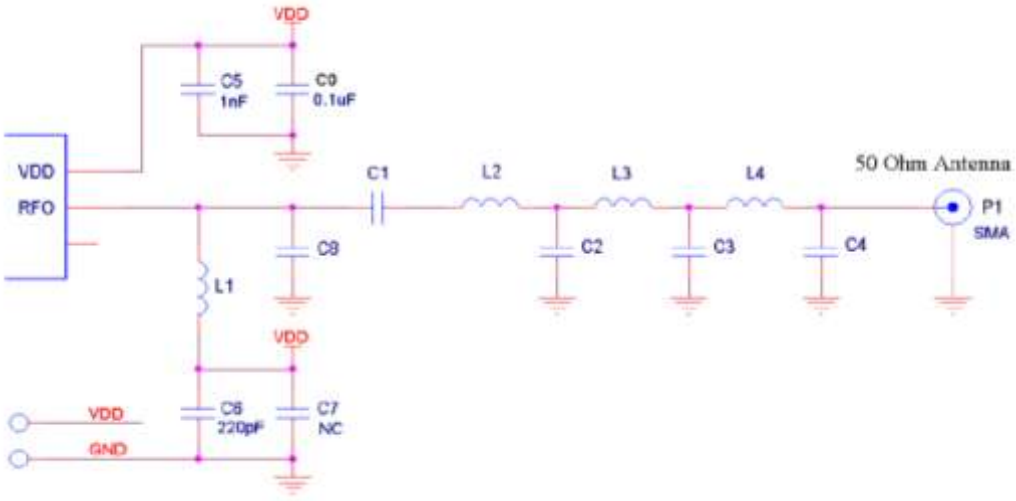

Figure 3. Low-pass Filter Networks Meeting ETSI/FCC/3C Certifications

Table 3. Matching Network Component Value Meeting ETSI/FCC/3C Certifications

Product Model	Frequency (MHz)	L1 (nH)	C1 (pF)	L2 (nH)	C2 (pF)	L3 (nH)	C3 (pF)	L4 (nH)	C4 (pF)	Notes
CMT211xA	315	180	68	62	18	27	27	27	9.1	3C standard
	315	180	68	62	18	27	18	330	-	FCC standard
	433	180	68	36	15	18	15	330	-	3C/FCC/ETSI standard
	868	100	68	8.2	9.1	8.2	8.2	220	-	ETSI standard
	915	100	68	5.6	10	8.2	5.1	220	-	FCC standard
CMT215xA CMT218xA	315	180	68	51	18	27	22	27	9.1	3C standard
	315	180	68	51	18	27	15	330	-	FCC standard
	433	180	68	36	15	18	15	330	-	3C/FCC/ETSI standard
	868	100	68	5.6	10	6.8	6.8	220	-	ETSI standard
	915	100	68	5.1	9.1	6.8	6.2	220	-	FCC standard

Notes:

1. In general, a 5th order filter is enough to meet application certification requirements except 7.5 MHz applications meeting the 3C standard, where a 7th order filter is required. For unified-design purpose, the reference-design DEMO board uses a 5th order filter where L4 is arranged in the following way.

   1) It is not necessary to reserve the L4 pad in the actual design;

   2) The reserved L4 pad can be connected using 330 pF/220 pF or alternatively using a 0 Ω resistor short or a transmission line.

2. The matching network component specifications in the DEMO board are as follows:

1) Capacitance: ±5%, 0402 NP0, 50 V.

2) Inductance: ±5%, 0603, Q>8 @ 10 MHz multilayer chip inductor.

3. For antennas with different impedances, housing structures, or PCB designs, the component values of the matching network may change. They need to be debugged under specific application conditions.

1.1.2 Low-cost RF Output Design

A 3rd order filter is used for low-cost applications as shown in the below figure.

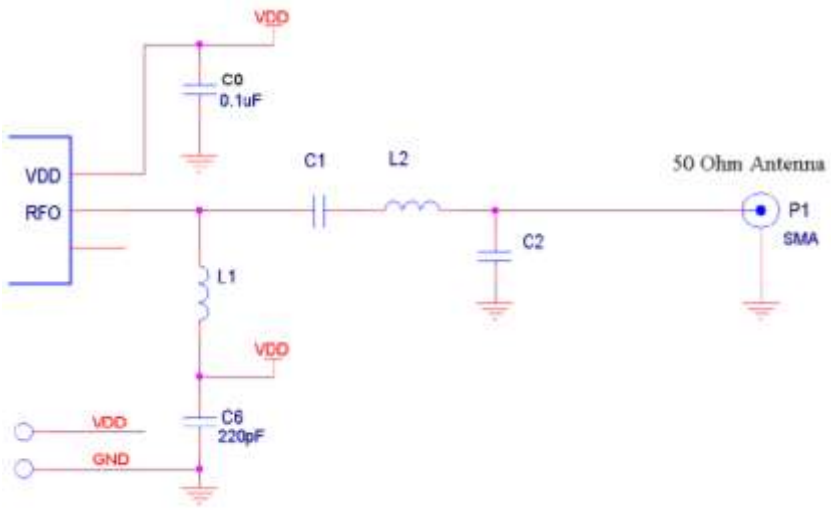

Figure 4. Low-cost Matching Network

Table 4. Component Value of Low-cost Matching Network

Product Model	Frequency (MHz)	L1 (nH)	C1 (pF)	L2 (nH)	C2 (pF)
CMT211xA	315	180	82	47	10
	433	180	82	27	9.1
	868	100	82	8.2	3.9
	915	100	82	6.8	3.9
CMT215xA CMT218xA	315	180	82	39	9.1
	433	180	82	22	9.1
	868	100	82	5.1	3.9
	915	100	82	4.3	4.3

Notes:

1. The matching network component specifications are:

    1) Capacitance: ±5%, 0402 NP0, 50 V.

    2) Inductance: ±5%, 0603, Q>8 @ 10 MHz multilayer chip inductor.

2. For antennas with different impedances, different housing structures, or different PCB designs, the component values of the matching network may change. They need to be debugged under specific application conditions.

1.1.3 Layout Design of Single-ended RF Output

As an example, for the CMT211xA-EM, the layout of the single-ended RF output is shown below.

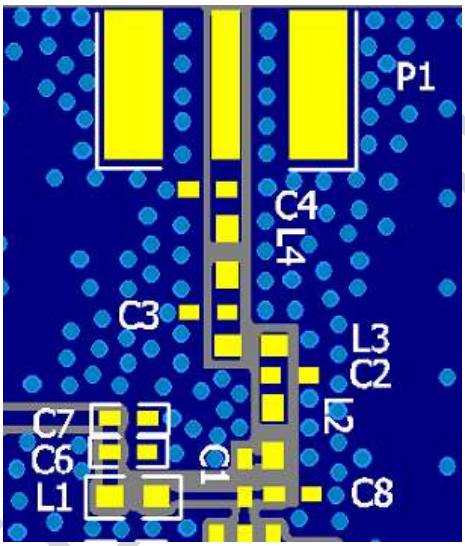

Figure 5. Layout Design Reference of Single-ended RF Output

Notes:

1. Keep the RF signal path as short and straight as possible to reduce RF signal loss.
2. Adjacent inductors should not be placed in a line to prevent coupling between them.
3. Place L1 as close as possible to the RFO pin.
4. Place the entire matching network as close as possible to the transmitting chip.
5. Due to the high output impedance of the chip pin RFO, a 0.2 mm wide transmission line is used between RFO and L2 in the reference design. The SMA connector is connected to the 50 Ω antenna, and a 1 mm transmission line is required behind L2.
6. Try not to have silk screen on the RF devices and traces. Thick silk screen will affect the dielectric constant and RF output impedance of the PCB.
7. The floor and RF traces should be as flat as possible to reduce impedance fluctuations on the transmission line.
8. As a commonly used antenna, the 1/4 wavelength (λ/4) monopole antenna is an effective half-wavelength (λ/2) antenna,

formed half by a 1/4 wavelength antenna and half by a ground plane that is equivalent to another 1/4 wavelength antenna. Therefore, the performance of a a monopole antenna design depends on the size of the ground plane placement. Considering different factors such as cost, performance, time to market, etc., users can choose different types of monopole antennas, such as PCB antennas, patch antennas, glue stick antennas, and wire antennas. In this reference design, P1 is an SMA connector for connecting the antenna, and the connector is connected to a 50 Ω impedance glue rod antenna to make the reference design gain optimum performance.

9. The reference layout of a PCB Loop antenna is shown in the below figure. The design considerations are as follows.

1) The PCB antenna should be placed as far as possible from the ground, and the line width should be at least 1 mm. The purpose is to reduce distribution parameters and improve radiation efficiency;

2) PCB Loop antenna should trace a complete circle to make the radiation area of the antenna as large as possible (this is mainly applicable to antenna design with a small PCB area).

3) Place the crystal trace as close as possible to the XTAL pin and place it as far away as possible from the antenna to avoid spur and self-excitation.

4) Design the position of an optional ground-to-ground capacitor (C9 in Figure 2) at the end of the antenna to optimize the transmission power.

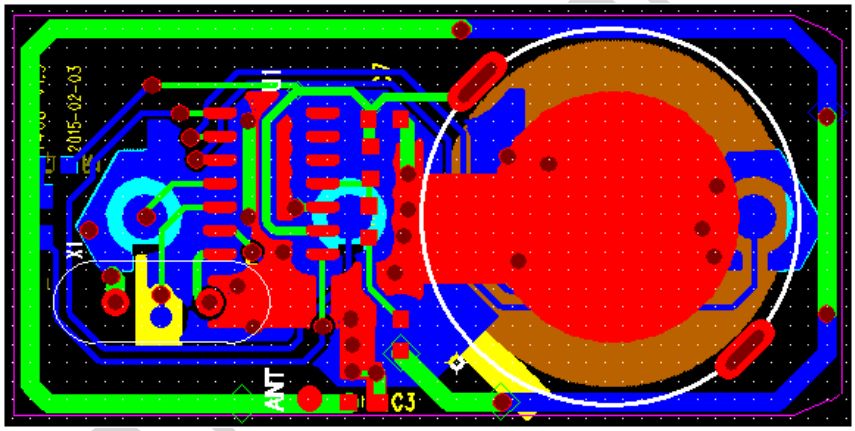

Figure 6. PCB Loop Antenna Layout Design Reference for Single-ended RF Output

1.2 Differential RF Output Circuit Design

1.2.1 Differential RF output Schematic Design

The CMT218xA supports differential RF output. The schematic is shown in the below figure. This section focuses on the differential RF output design of the CMT218xA. Other circuit parts design are covered in other corresponding sections.

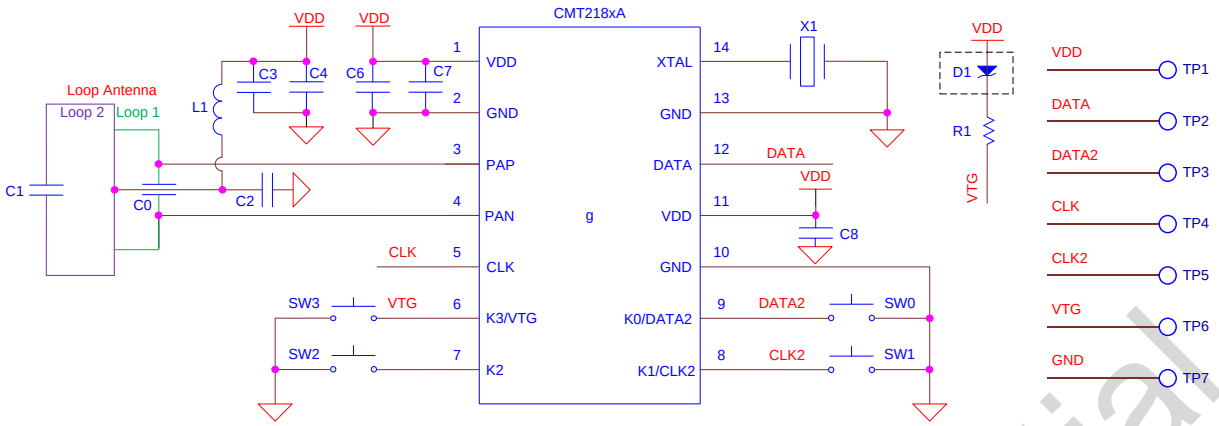

Figure 7. CMT218xA Differential RF Output Schematic Design

Notes:

1. C1 is a resonant capacitor used to resonate the main loop of the tap loop antenna to the RF frequency.

2. C2 is a filter capacitor filtering out the phase offset between the differential output ports to improve the output power efficiency.

3. C0 is an optional compensation capacitor. When the built-in tuning capacitor is insufficient, C0 can be used as external compensation.

4. L1 is an energy absorbing inductor (choke inductor).

5. Users can change the transmission power in 2 ways.

   1) Set the Tx power parameter through the USB Programmer and RFPDK to change the chip transmission power.

   2) Place a resistor (not shown in the above figure) between the energy absorbing inductor and the power supply to adjust the transmission power via changing the resistance value. Due to the presence the resistor, this method will reduce transmission efficiency. So it is recommended to change the transmission power through changing the chip's transmission power setting.

6. The differential RF output uses a loop antenna. The below 2 kinds of antennas are commonly used.

   a) Single loop antenna. The loop antenna is equivalent to an inductor that resonates with the internal capacitance of the chip at the RF frequency. The internal capacitance of the chip can be adjusted from 0.1 pF to 6 pF with corresponding the range of CCode on the corresponding RFPDK as 1~127. The optimum value at 433 MHz is usually around 100, and the optimum value at 868 MHz is around 70. After determining the capacitance, users can calculate the resonant inductance value according to the operating frequency, then obtain the size of the loop antenna through the antenna calculation formula. However, the disadvantages of this type of antenna are as follows.

      1) The equivalent impedance is high (a few dozens of kΩ), which does not match the internal impedance of the chip, resulting in low radiation efficiency.

      2) The Q value is high and it is easy to result in mismatching due to the influence of the external environment.

   b) Tap loop antenna. Against the disadvantages of single-loop antennas, namely high equivalent impedance, users can change the impedance of the antenna to the optimal equivalent impedance (about 500 Ω) by changing the tap point between the two rings to achieve optimal impedance matching. In the tap loop antenna, Loop1 is a resonant ring, which is resonant with the internal capacitance of the chip at the RF frequency. The design method is the same as that of the single loop antenna. Loop2 is a radiating loop, which determines the radiation efficiency of the tap loop antenna and forms a series resonance with C1. The larger the size, the better the radiation effect and the greater the equivalent inductance. The impedance conversion ratio will also change accordingly. Generally users can select the optimal tap

point to achieve the optimal performance by using simulation software or debugging in lab,.

As an example, for the CMT2180A-EM-D (433.92 MHz), the designed antenna size is shown in the below figure and the component value of related material BOM is listed in the below table.

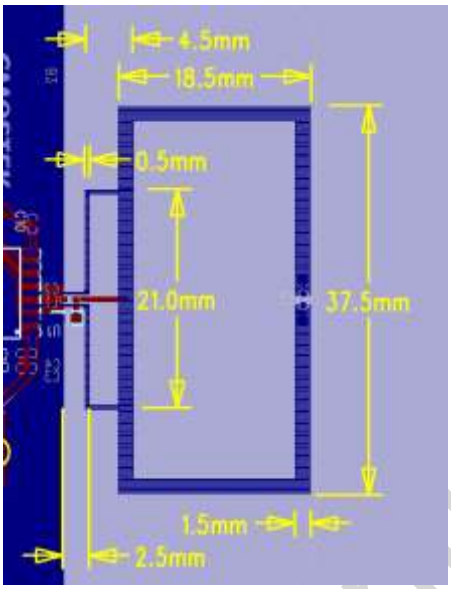

Figure 8. Differential RF Output Layout Reference Design for CMT2180A-EM-D @ 433.92 MHz

Table 5. Differential RF Output Matching Network Design @433.92 MHz

Product Model	Operating Frequency（MHz）	L1（nH）	C1（pF）	C2（pF）
CMT218xA	433.92	180	2.2	2.2

1.2.2 Differential RF Output Layout Design

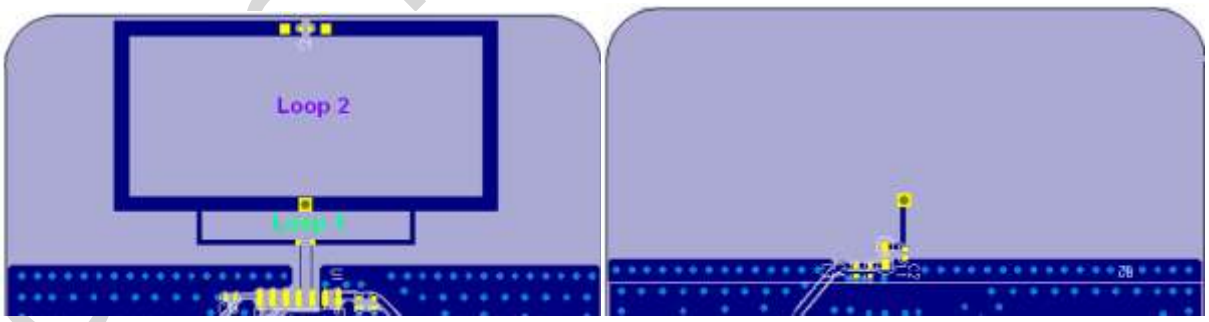

Figure 9. Differential RF Output Layout Design Reference

Notes:

1. Loop1 and Loop2 need to be physically symmetrical as much as possible. C2 placed on the back side is to filter out the mismatched phase component between the differential outputs to optimize output efficiency.
2. The energy absorbing inductor L1 and its decoupling capacitor C3/C4 are placed on the back side as close as possible to the PAP/PAN pin.

3. There should be enough clearance around the differential PCB antenna, with no ground plane and other trace arrangement.
4. When the size of the loop antenna (Loop2) increases, the transmission efficiency of the RF signal will increase and the resonant frequency will decrease, In practical applications, the actual size of the loop antenna is determined by the application housing design. Therefore, the size of a suitable loop antenna should be a balance among transmission efficiency, resonant frequency and housing design. In this reference design (EM board), the loop antenna is implemented using a 1.5 mm wide, λ/4 long PCB wire.
5. Try not to have silk screen on RF devices and traces. Heavy silk screen will affect the dielectric constant and RF output impedance of the PCB.
6. The ground plane and RF traces should be as flat as possible to reduce impedance fluctuations on the transmission line.

2 Crystal Circuit Design

The CMT211x/5x/8xA supports single-ended crystal design with crystal load capacitors integrated into the chip and no need for additional load capacitance. The recommended crystal specifications are listed in the below table.

Table 6. Crystal Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Crystal frequency[1]	F_{XTAL}			26		MHz
Crystal frequency tolerance[2]	ppm			20		ppm
Load capacitance	C_{LOAD}			15		pF
ESR	Rm			60		Ω
Crystal startup time[3]	t_{XTAL}			400		us

Notes:

[1]. For CMT211x/5x/8xA, an external 26 MHz reference clock can be used to drive the XI pin directly through a coupling capacitor. The peak-to-peak level of the external reference clock is required between 0.3 and 0.7 V.

[2]. It involves:(1) initial tolerance, (2) crystal loading, (3) aging, and (4) temperature changing. The acceptable crystal frequency tolerance is subject to users' product communication system requirements such as frequency, channel, bandwidth, etc.

[3]. The required crystal load capacitance is integrated in the chip to reduce the number of off-chip components.

[4]. This parameter is to a large degree crystal dependent.

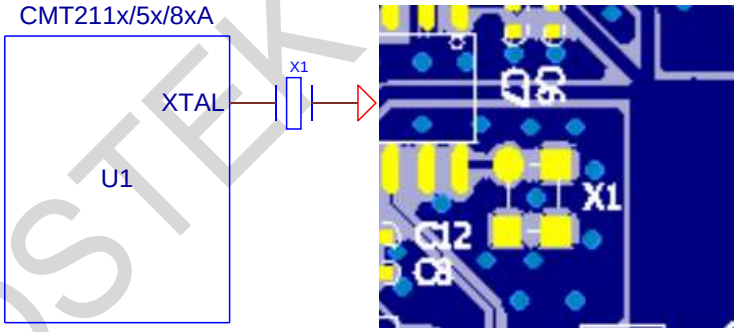

Figure 10. Schematic (left) and Layout (right) Design of Single-ended Crystal

Notes:

1. The crystal should be placed as close as possible to the CMT211x/5x/8xA to reduce trace parasitic capacitance, which helps reduce potential frequency deviation effectively.

2. The crystal should be placed as far away as possible from the PA output, antenna and digital trace. In addition, place ground plane around as large as possible. These can help reduce the potential output interference of the crystal back PA effectively.

3. Ground the metal casing of the crystal (for example, 49S plug-in crystal, or column crystal, etc.)

4. The crystal load capacitance (15 pF by default) is integrated in the chip , which does not require external load capacitors. Users can select the crystal with a frequency of 26 MHz and a load capacitance of 15 pF. For safety consideration, it is recommended that users reserve test points on the PCB to fulfill the online modification of chip parameters. See Section 8 for details.

3 Digital Signal Design

Please be noted the following digital signal trace considerations.

1. Digital signal traces should be as far away as possible from the RF and crystal trace areas.
2. Place areas of ground plane as large as possible around digital signals to reduce crosstalk.

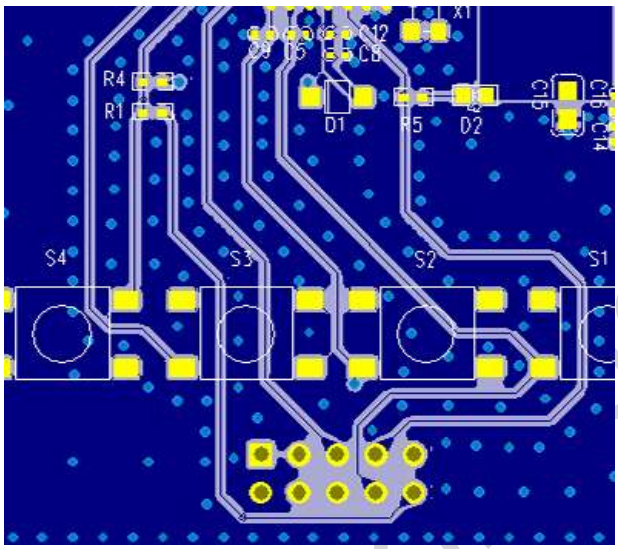

Figure 11. Digital Signal Layout Design

4 Power Supply and Ground Design

4.1 Power Supply Filtering Circuit Design

To reduce the noise/ripple-caused impact on the chip power supply and the effect of the PA output on the power supply, users should design a filtering capacitor at the 2 points as shown in the below figure.

1. At the VDD pin of the chip (C0/C5).

2. At the point where the energy absorbing inductor of the RFO or PAP/PAN output pin connects to one end of VDD (C6/C7).

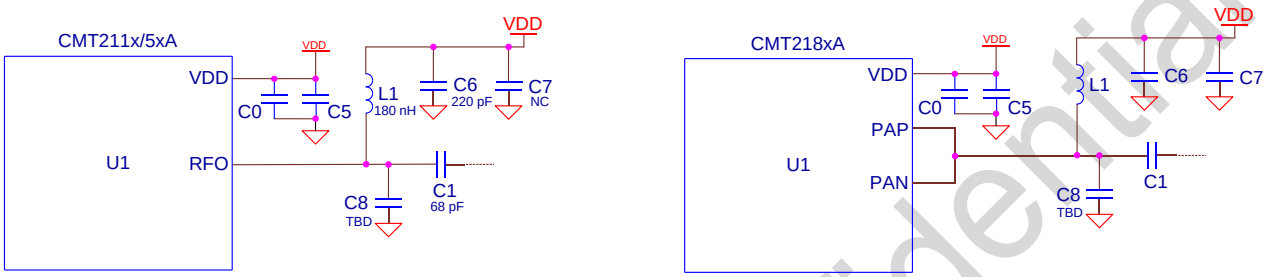

Figure 12. VDD and RF Output Filtering Capacitor Design

Notes (for layout design):

1. Place the C6/C7 layout as close as possible to the energy absorbing inductor L1.

2. Try to place the C0/C5 layout as close as possible to the VDD pin of the chip.

4.2 Ground Design

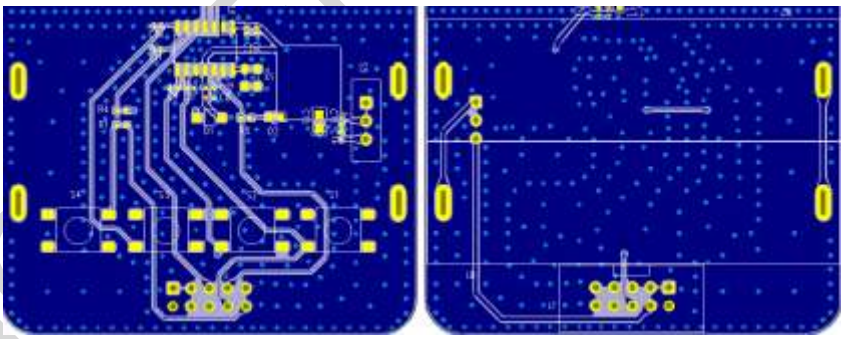

Figure 13. Ground Plane Design

Notes:

1. Place areas of ground plane as large and continuous as possible.

2. To reduce the EMI radiated by the power supply loop externally, the ground trace design should in best effort minimize the space of the path through which the current loop backs to the power supply.

3. Place a ground plane as large as possible under the chip to reduce the impact on the continuity of the RF output transmission line impedance and improve the ESD performance.

4. Make as many as possible vias with a diameter no more than λ/10 on the PCB edges to reduce high harmonic radiation on the PCB edges.

5. Make sure to place ground plane under the chip.

5 Power Optimization Considerations

In transmission applications where power consumption is critical, the CMT211x/5x/8xA offers a variety of methods to meet requirements of different application scenarios including:

1. Reduce the transmission power.
2. Optimize the matching network.
3. Increase the transmission data rate.
4. Increase the packet interval.
5. Control the LED drive current.
6. Use a differential RF output.

5.1 Reduce Transmission Power

Users can reduce chip power consumption effectively by setting a smaller transmission power value on the RFPDK. However, as the transmission distance is reduced accordingly with the transmission power reducing, users need to have a balance between power consumption and transmission distance to make sure, with the reduced power consumption, the transmission distance can still meet the system requirements. Otherwise, users may need to consider other methods to optimize either power or distance.

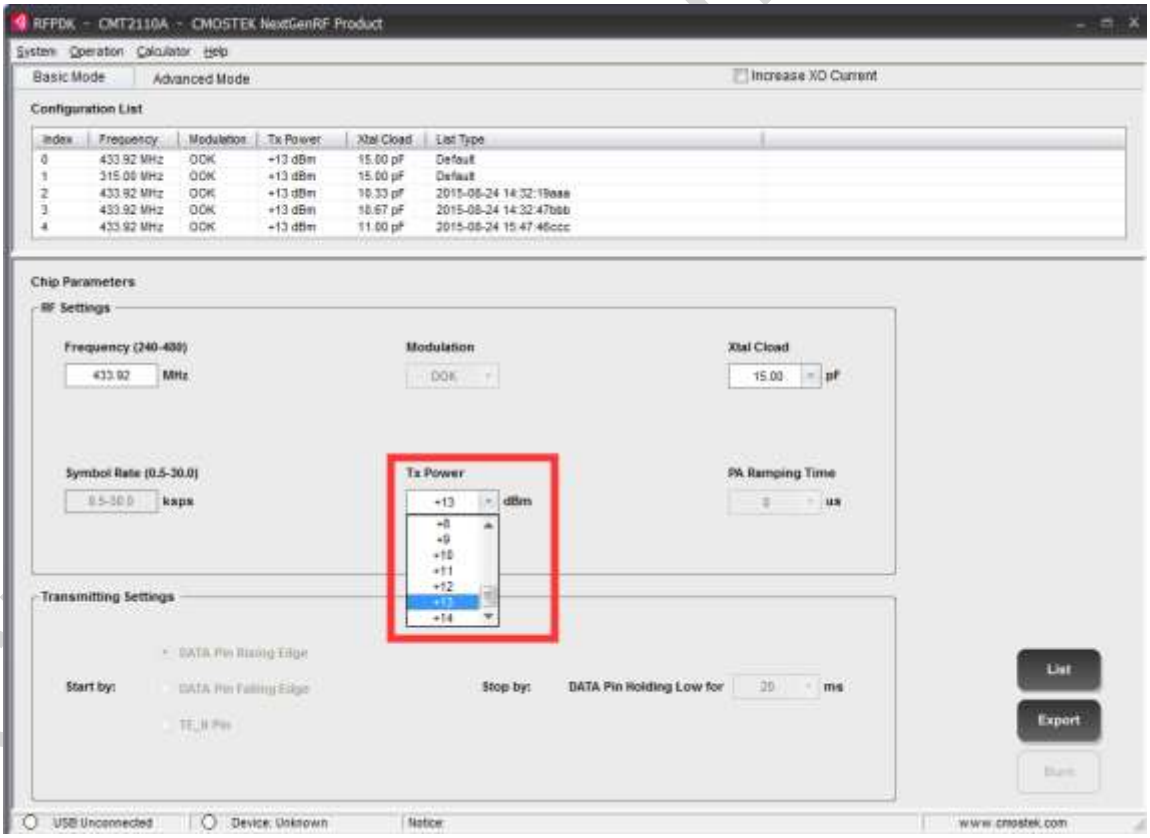

Figure 14. Change Chip Transmission Power with RFPDK

Please be noted that connecting a current limiting resistor to the energy absorbing inductor cannot reduce the chip power consumption effectively. Reducing the transmission power by changing the chip settings is recommended instead .

5.2 Matching Network Optimization

The purpose of the matching network is to match the output impedance to the antenna impedance. Improper impedance will reduce the transmission efficiency and waste power. Users should design the matching networks that are optimized for specific applications using network analyzers according to different antennas, thus to improve transmission efficiency and optimize transmission power.

Moreover, it should be noted that reducing the order of the matching network filter can also help improve transmission efficiency and reduce power consumption, however, the reduction of the filter order results in the reduction of harmonic suppression as well, so this method is suitable for applications with no critical requirements on harmonic emission.

5.3 Increase Transmission Data Rate

With the same packet interval, increasing transmission data rate can shorten the time of packet transmission, thereby reducing the average power consumption.

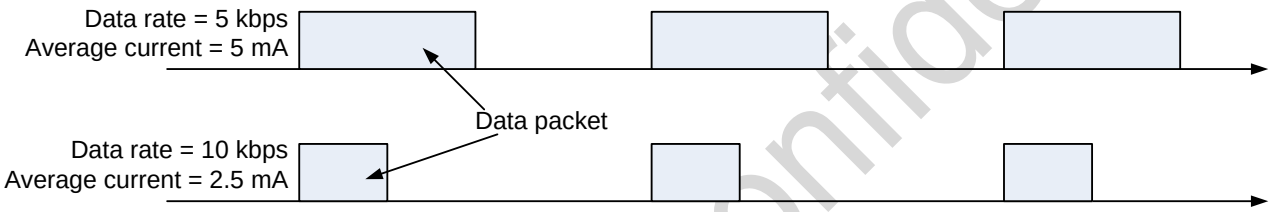

Figure 15. Reduce Average Power Consumption by Increasing Data Rate

The CMT211xA supports to control the end of transmission via TWI thus to support immediate transmission start/stop for further power saving.

It should be noted that the increase in data rate may reduce the receiving sensitivity and then impact the transmission distance further.

5.4 Increase Interval Between Packets

Another way to reduce average power consumption is to increase the packet interval to reduce the average power consumption as shown in the below figure.

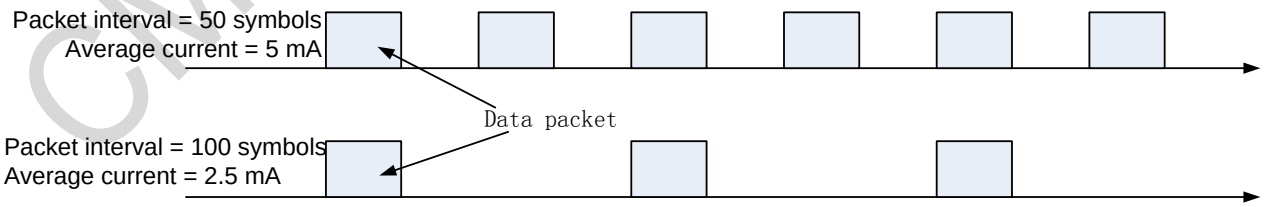

Figure 16. Increase Packet Interval to Reduce Average Power Consumption

The CMT211x/8xA can set the packet interval through the MCU program. The CMT215xA can set the packet interval through RFPDK as shown in the following figure.

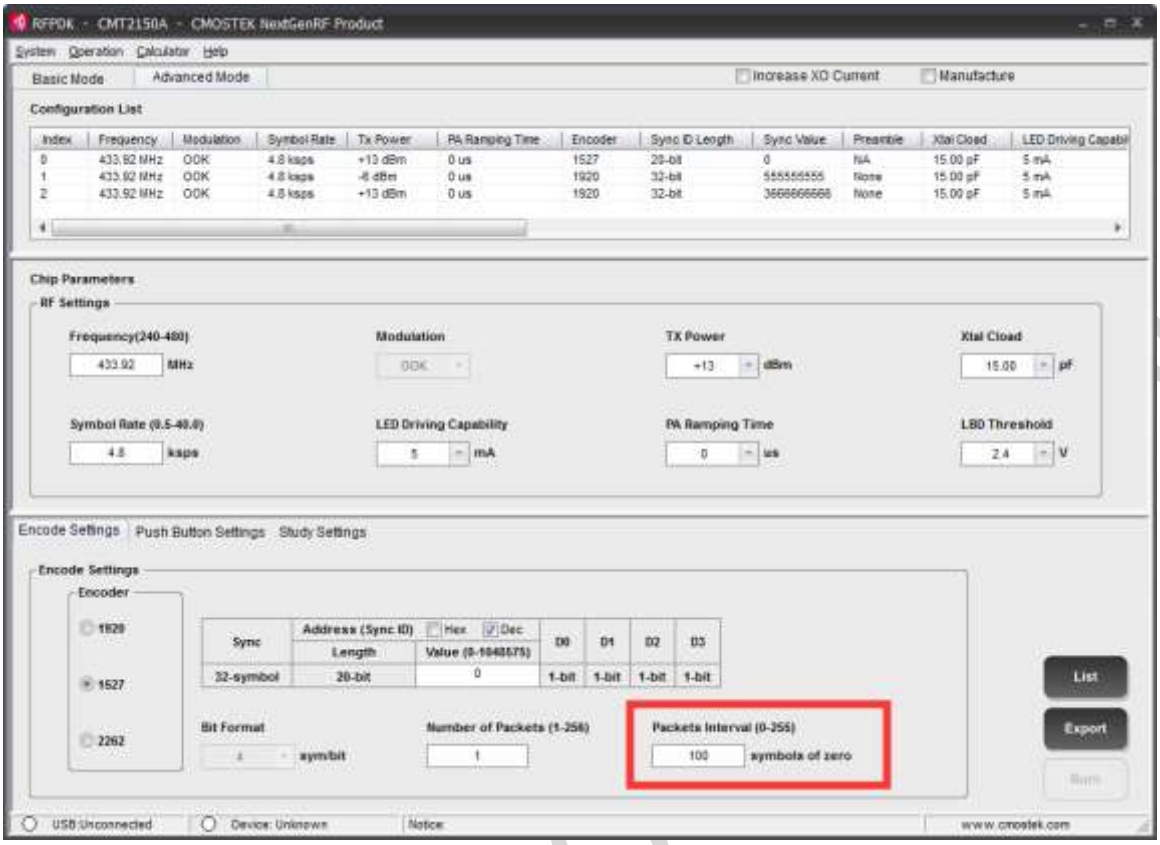

Figure 17. Setting Packet Interval for CMT215xA on RFPDK

It should be noted that this method is more suitable for applications transmitting multiple data packets at a time, such as doorbell applications and remote control applications. Users need to ensure that, for the increased packet interval, the receiving window of the receiving side is long enough to receive the correct data packet reliably. The unit set in the *Packet Interval* in the above figure is symbol, and the length of the symbol is determined by the symbol rate. For example, when the symbol rate is 5 ksps, the length of each symbol is 200 us, and the total length of 100 *symbols of zero* is 200 us * 100 = 20 ms.

5.5 Drive Current of Control LED

The CMT215xA can drive the LED to indicate transmission state or low voltage state. A series current limiting resistor is placed between LED and VDD to minimize the current consumed by the driving LED while ensuring acceptable LED brightness.

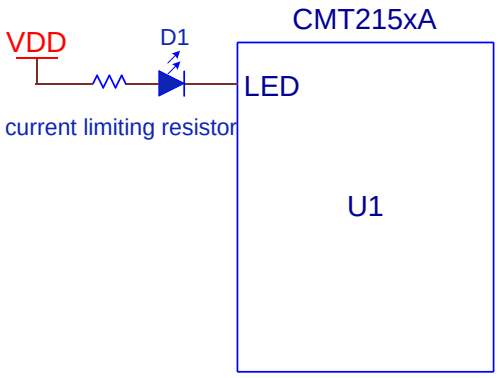

Figure 18. Drive Current of Control LED

Note that, in RFPDK , the parameter *LED Driving Capability* is for limiting the maximum driving capability. In case of driving current below this driving capability value, users need to use a current limiting resistor to control the driving current.

5.6 Using Differential RF Output

In addition to supporting single-ended RF outputs, the CMT218xA can also support differential RF outputs, as described in Section 2.2. Differential antennas have better performance on power consumption.

Table 7. Crystal Oscillator Specification

Transmission Power	Single-end RF Output Power Consumption (mA)	Differential RF Output Power Consumption（mA）
0 dBm	8.5	4.5
+10 dBm	11.5	6.9
+13 dBm	13.0	9.1
Notes: [1]. The above power consumption is obtained under the conditions of OOK and 50% duty-cycle.		

6 Press-Key Circuit Design

The CMT215xA supports combination key. When combination key is required, an isolation diode is placed between the combined keys and the pins for isolation purpose to prevent a single key interfere with other keys as shown in the below figure.

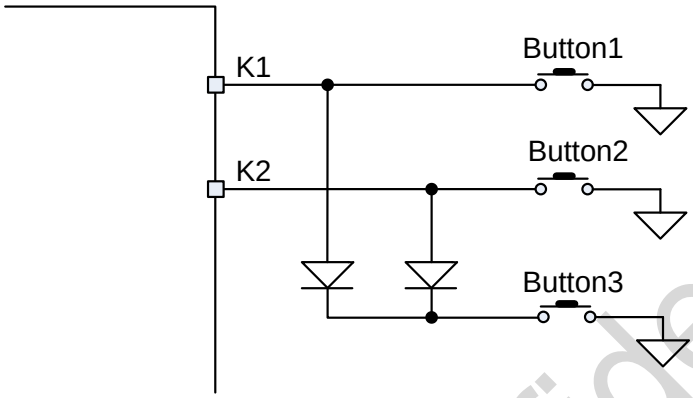

Figure 19. Combination Key Design

The CMT218xA supports combination key as well, however whether isolation diodes are required for isolation purpose depends on the design of the corresponding MCU program.

7 Test Circuit Design

The CMT series chips enrich the functionality for users to change chip function through chip programming. Therefore, CMOSTEK strongly recommends users reserve test points for the chip when designing the PCB, which helps in the below aspects.

1. It is convenient to change chip functions in production.

2. It is convenient to get chip configuration information by reading the chip configuration.

The test points need to be reserved are listed in the below table according to different product models.

Table 8. Crystal Oscillator Specification

Product Model	Reserved Test Pin [1]
CMT211x/5xA	DATA, CLK
CMT218xA[2]	DATA, DATA2, CLK, CLK2, VTG
Notes: [1]. VDD and GND are not included in above test points. During chip testing or programming, the chip need to be in operating state. [2]. The 15 V voltage is needed for VTG programming. Therefore, the protection diode D1 should be placed between VTG and the chip's VDD for isolation, as shown in the below figure.	

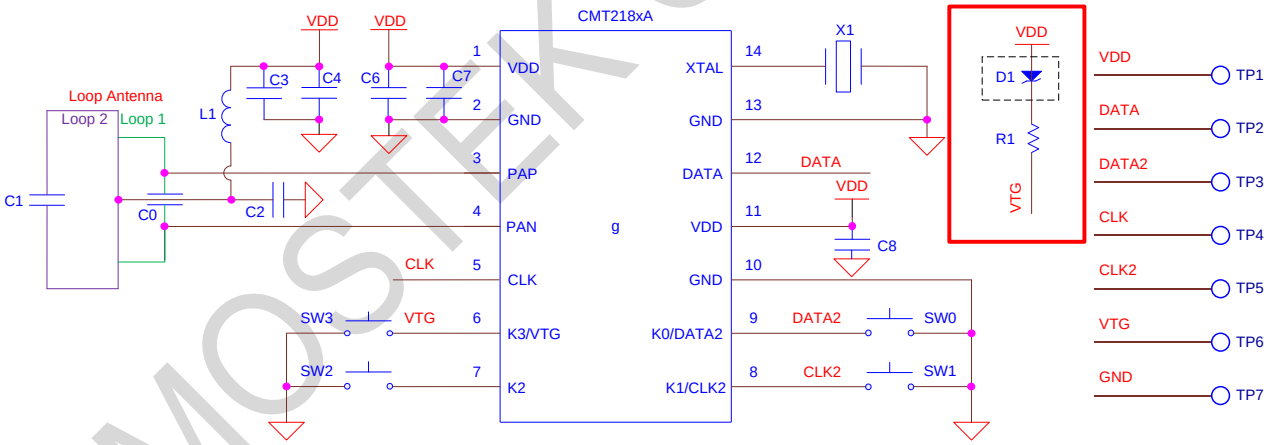

Figure 20. Isolation Design between VTG and VDD

8 Design Checklist

Users can check the actual design with the below checklist to make sure they are well considered.

Table 9. Design Checklist

Single-ended RF Output Design	
☐	Whether the PAP/PAN pins are connected together when the CMT218xA is used as a single-ended RF output.
☐	Whether the RF signal path is as short as possible to reduce the RF signal loss.
☐	Whether avoid to place adjacent inductors in the same direction to avoid mutual coupling.
☐	Whether the energy absorbing inductor L1 is placed as close as possible to the RFO pin or PAP/PAN.
☐	Whether consider the impedance value when selecting RF transmission line trace width (select 1 mm wide transmission line for a impedance of about 50 Ω).
☐	Whether the entire matching network is placed as close as possible to the transmitting chip.
☐	Whether try to prevent silk screen printing on RF devices and traces
☐	Whether the ground plane and RF trace are as flat as possible.
☐	Whether the length of the antenna is close to λ/4.
☐	Whether the crystal is as far away as possible from the antenna.
☐	Whether the PCB antenna width is more than 1 mm.
☐	For PCBLoop antenna, whether the PCB antenna goes a complete circle along the PCB frame to increase the radiation area when the PCB area is small.
☐	For PCBLoop antenna, whether an optional ground capacitance is added to the end of the PCB antenna.
Differential RF Output Design	
☐	Whether the resonant ring (Loop1) and the radiating ring (Loop2) are physically symmetrical.
☐	Whether the energy absorbing inductor L1 and its filter capacitor are as close as possible to the PAP/PAN pin.
☐	Whether there is enough clearance area near the differential antenna with no ground plane and no trace.
☐	Whether the area of the radiating ring (Loop2) is as large as possible (the circumference is close to λ/4 and the line width is is more than 1.5 mm).
☐	Whether the area of the resonant ring (Loop1) makes the reading value of CCode on RFPDK around 100.
☐	Whether the position of the optional compensation capacitor C0 is reserved on the resonant ring (Loop1) and the physical symmetry is ensured.
☐	Whether try to prevent silk screen printing on RF devices and traces.
☐	Whether the ground plane and RF trace are as flat as possible.
☐	Whether the parasitic parameters introduced by the chip housing is taken into account when designing and debugging the matching network.

Crystal Circuit Design	
☐	Whether the crystal is placed as close as possible to the CMT211x/5x/8xA to reduce the trace parasitic capacitance, which can reduce potential frequency error efficiently.
☐	Whether the crystal circuit is placed as far away as possible from the PA output, antenna or digital trace and whether areas of ground plane are placed as large as possible around the crystal circuit, which can effectively reduce the potential output interference of the crystal back PA.
☐	Whether the metal casing is grounded, e.g. for 49 S plug-in crystal, or column crystal.
Digital Signal Design	
☐	Whether the digital signal is placed as far away as possible from the XTAL and RF trace.
☐	Whether ground plane are as large as possible around digital signals to reduce crosstalk.
Power and Ground Design	
☐	Whether the VDD filter capacitor C0/C5 layout is placed as close as possible to the VDD pin of the chip.
☐	Whether the inductive filter capacitor C6/C7 layout is placed as close as possible to the energy absorbing inductor L1.
☐	Whether areas of ground plane are placed as large and continuous as possible.
☐	Whether the ground trace design minimizes the space of the path through which the current loop backs to the power supply, to reduce the EMI radiated externally from the power supply loop.
☐	Whether the bottom of the chip is grounded as much as possible to reduce the influence on the impedance continuity of the RF output transmission line and enhance the ESD performance.
☐	Whether place as many as possible vias with a diameter no more than λ/10 on the PCB edges to reduce the higher harmonic emissions from the PCB edges,.
☐	Whether ground plane is placed under the chip.
Press-key Circuit Design	
☐	For CMT215xA, whether combination keys are isolated through isolation diodes.
Test Circuit Design	
☐	Whether the test programming point is reserved in the PCB design.
☐	For CMT218xA, whether the protection diode D1 is designed when the VTG programming is required.

9 Revise History

Table 10. Revise History Records

Version No.	Chapter	Description	Date
0.8	All	Initial version	2015-09-16
0.81	Overview	Change product model list: change item 6 from CMT2110A to 2180A	2019-10-14

10 Contacts

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