CMOSTEK

AN170

CMT2110B/CMT2117B User Guide for Schematic and PCB Layout Design

Overview

This document provides the schematic and PCB layout design guidelines for users engaging in the development based on the CMT2110B/CMT2117B transmitter chip, which is part of the CMOSTEK NextGenRF™ product family. The document aims for guiding users to quickly achieve target performance objectives such as improving output power, efficiency, transmission current, and reducing system cost, spurious emission.

The part numbers covered in this document are shown in the table below.

Table 1. Part Numbers Covered in This Document

Part Number	Frequency (MHz)	Modulation Method	Chip Function	Max. Output Power	Packaging
CMT2110B	312 - 480	OOK	Transmitter only	+13 dBm	SOT23-6
CMT2117B	624 - 960	OOK	Transmitter only	+13 dBm	SOT23-6

This document will discuss in the following aspects the usage of CMOSTEK NextGenRF™ CMT2110B/CMT2117B transmitter-only series chips.

- Application circuit design
- PCB layout design
- Crystal circuit design
- Digital signal design
- Power supply and ground design
- Design checklist

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1. Application Circuit Design

CMT2110B/17B is a direct-mode RF transmitter with single-wire data input and single-ended RF output. Since the chip is pretty simple and easy in function, the circuit design focus more on RF impedance matching to gain high PA output power along with high overall efficiency. For products with safety certification requirements, it needs to apply a filter network with both low insertion loss and high out-of-band attenuation in order to lessen harmonics and spurs.

1.1 Typical Application

The typical application matching network in the figure below focuses on maximizing output power rather than optimizing harmonics and spurs. It applies 3rd order network to implement the impedance matching between antenna and RFO port to achieve the lowest cost and least components.

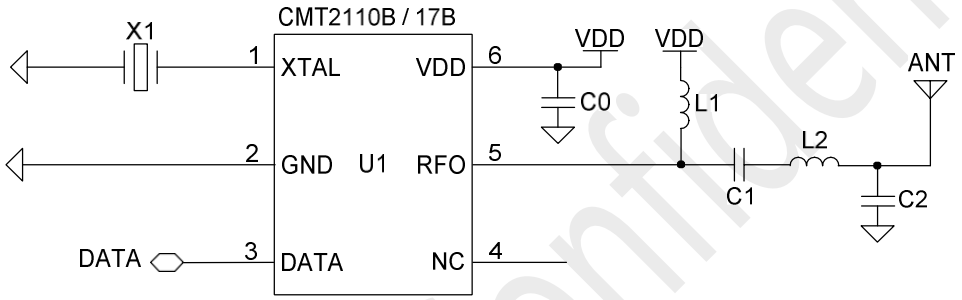

Figure 1. CMT2110B/17B Typical Application Schematic

Notes:

1. L1 is a choke inductor.
2. C0 is a power decoupling capacitor in order to reduce the impact of both PA output and power supply on the chip.
3. C1 is a DC blocking capacitor.
4. L2 and C2 form a matching network.
5. ANT is an antenna of 50 ohm.

Table 2. CMT2110B/17B Typical Application BOM

Label	Description	Component Value		Unit	Supplier
		433.92 MHz[1]	868.35 MHz[2]		
U1	CMT2110/17B, OOK transmitter	-		-	CMOSTEK
X1	±20 ppm, SMD32*25 mm crystal	26.2982	26.3136	MHz	EPSON
C0	±20%, 0402 X7R, 25 V	0.1		uF	
C1	±5%, 0402 NP0, 50 V	68	56	pF	
C2	±5%, 0402 NP0, 50 V	2.2	5.6	pF	
L1	±5%, 0603 multilayer chip inductor	180	100	nH	Sunlord
L2	±5%, 0603 multilayer chip inductor	27	7.5	nH	Sunlord

Notes:

[1]. Only CMT2110B supports 433.92 MHz applications.
[2]. Only CMT2117B supports 868.35 MHz applications.

2 types antennas are commonly used in many applications: λ/4 monopole antennas (PCB antennas, wire antennas, etc.) and PCB loop antennas. Subject to factors such as product size, PCB layout, casing, it is uneasy to simulate and measure the actual antenna impedance. It's not that easy either to purchase antennas with inductor and capacitor values conforming specifications. So, it is recommended that if the antenna impedance is uncertain, reserve the same LC network after L2, C2 as shown in the above figure, which makes it more flexible to debug impedance matching parameters and more easier to achieve favorable output power.

1.2 Typical Application for ETSI/FCC Compliance

Standards such as ETSI/FCC/3C have strict requests on emission and spurs. CMOSTEK recommends 5 to 7-order low-pass filter networks for matching, as shown in the figure below.

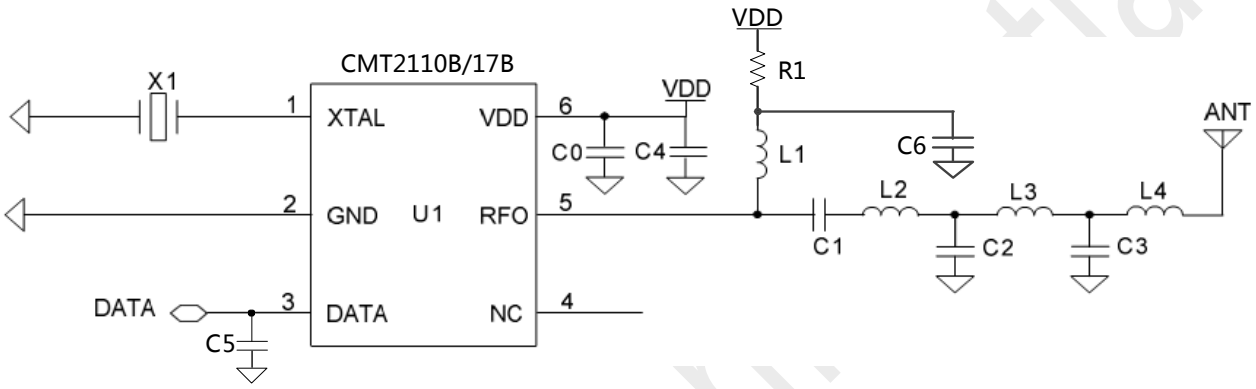

Figure 2. CMT2110B/17B Typical Application Schematic for ETSI/FCC Compliance

Notes:

1. L1 is a choke inductor.
2. C0, C4 are power decoupling capacitors to reduce the impact of both PA output and power supply on the chip.
3. C1 is a DC blocking capacitor.
4. L2, C2, L3, C3 and L4 form a low-pass filter matching network.
5. ANT is an SMA connector. In this example, an antenna of 50-ohm is used.
6. C5 and C6 are decoupling capacitors. R1 is the resistor to adjust output power.

Table 3. CMT2110B/17B Typical Application BOM for ETSI/FCC Compliance

Label	Description	Component Value		Unit	Supplier
		433.92 MHz[1]	868.35 MHz[2]		
U1	CMT2110/17B, OOK transmitter	-		-	CMOSTEK
X1	±20ppm, SMD32*25 mm crystal	26.2982	26.3136	MHz	EPSON
C0	±20%, 0402 X7R, 25V	0.1		uF	
C1	±5%, 0402 NP0, 50V	18	15	pF	
C2	±5%, 0402 NP0, 50V	4.3	4.3	pF	
C3	±5%, 0402 NP0, 50V	4.3	2.2	pF	
C4	±5%, 0402 NP0, 50V	220	220	pF	
C5	±5%, 0402 NP0, 50V	27	27	pF	
C6	±5%, 0402 NP0, 50V	1000	1000	pF	

R1	Resistor, 5%，1/8W，0603	0 - 2200	0 - 2200	Ω	
L1	±5%, 0603 multilayer chip inductor	180	100	nH	Sunlord
L2	±5%, 0603 multilayer chip inductor	51	12	nH	Sunlord
L3	±5%, 0603 multilayer chip inductor	47	15	nH	Sunlord
L4	±5%, 0603 multilayer chip inductor	36	15	nH	Sunlord

Notes:

[1]. Only CMT2110B supports 433.92 MHz applications.

[2]. Only CMT2117B supports 868.35 MHz applications.

2. PCB Layout Design

Let's take CMT2110B/17B-EM typical schematic (refer to Figure 2) and its PCB layout as an example to specify the design considerations. CMT2110B/17B-EM applies 2-layer layout design. The top layer and bottom layer layouts are shown in the figure below.

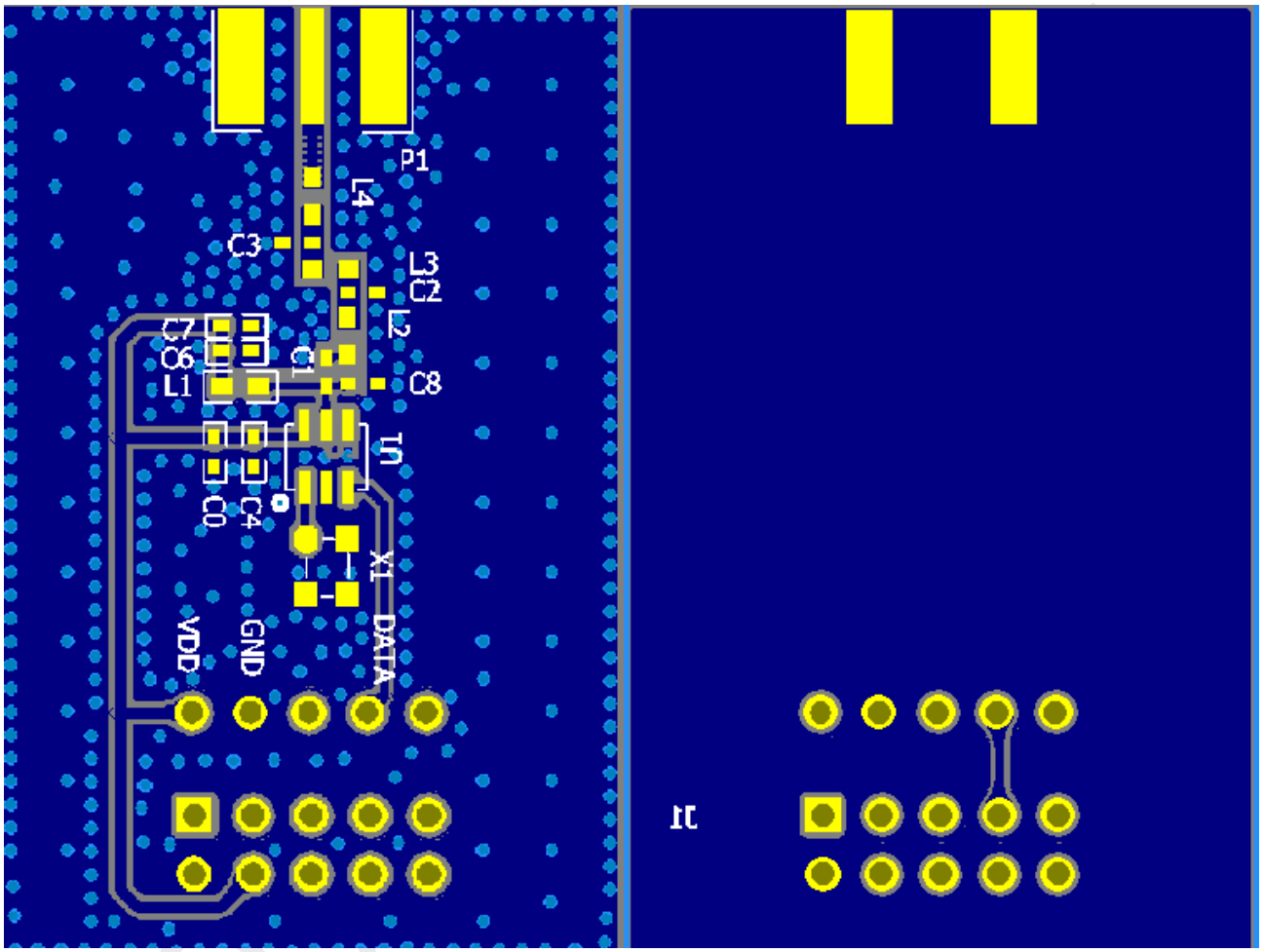

Figure 3. CMT211 CMT2110B/17B-EM PCB Layout

Notes:

1. The RF signal path should be as straight and short as possible to reduce the RF signal loss of input and output.
2. The RF trace should be as flat as possible to reduce reflections caused by impedance fluctuations on the transmission line. In the above figure, the trace between L2 and P1 is a 50 Ω impedance transmission line. In this reference design, the 2-layer board applies FR4 board material; the dielectric constant Er is 4.6; copper thickness is 1 oz; the PCB thickness is 0.8 mm. When the width of the transmission line is about 1 mm, and the gap between the transmission line and the ground (GND) is set to 0.35 mm, a transmission line with an impedance of 50 ohms can be obtained.
3. Try not to have silk screen falling on the RF path. Silk screen will affect the impedance of the transmission line.
4. Place L1 as close as possible to the PA pin. Place adjacent inductors as orthogonal as possible to reduce mutual coupling.
5. The RF path, the crystal oscillator circuit, and the layer under the IC must have complete ground plane (GND).

3. Crystal Circuit Design

Table 4. Crystal Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Crystal frequency[1]	F_{XTAL}			-		MHz
Crystal frequency tolerance[2]				±20		ppm
Load capacitance	C_{LOAD}			22		pF
ESR	Rm				60	Ω
Crystal startup time[3]	t_{XTAL}			400		us

Notes:

[1]. It supports an external reference clock to drive the XTAL pin directly through a coupling capacitor. The peak-to-peak level of the external reference clock is required between 0.3 and 0.7 V.

[2]. It involves:(1) initial tolerance, (2) crystal loading, (3) aging, and (4) temperature changing.

[3]. This parameter is to a large degree crystal dependent.

Users should be noted the following considerations:

1. The crystal should be as close as possible to the IC to reduce the parasitic capacitance of the trace and reduce the frequency variance.
2. The crystal should be as far away as possible from the PA output, antenna, and digital tracing; and please place ground plane as much as possible around it. These can effectively reduce the interference to the crystal.
3. If a 49S plug-in crystal or columnar crystal is used, the metal casing of the crystal should be grounded.

4. Digital Signal Design

Please be noted the following digital signal DATA trace considerations.

1. Place areas of ground plane as large as possible around digital signals to reduce crosstalk.
2. Digital signal trace should be as far away as possible from the RF and crystal trace areas .

5. Power Supply and Ground Design

5.1 Power Supply Filtering Circuit Design

To reduce the impact on the chip caused by the noise/ripple of the power supply, and reduce the impact on the power supply caused by PA output, the decoupling capacitor should be placed close to the VDD pin and choke inductor of the chip.

5.2 Ground Design

Ground plane is important to improve RF performance and reliability. Users should take the considerations below into account.

1. Reference ground: the RF trace needs its adjacent layer to have a large continuous ground as a reference plane to achieve efficient power output.
2. Place ground plane alongside both sides of the RF trace and place vias to the reference ground plane to reduce spurious emission.
3. Place vias on the ground network of each layer to the reference ground to reduce the loop path, thereby reducing the emission of the loop.
4. On the PCB edges, place vias as many as possible with no more than λ/10 in size to reduce emissions and enhance ESD resistance capabilities.
5. Since the crystal circuit is sensitive to interference, place ground plane around it for isolation.

6. Design Checklist

Table 5. Design Checklist

RF Design	
☐	Whether the filter capacitor is as close as possible to the power supply pin of the chip.
☐	Whether the choke inductor is as close to the PA pin as possible.
☐	Whether the adjacent inductors have been avoided to be placed in the same direction.
☐	Whether the RF signal path is as short as possible.
☐	Whether the impedance size is well considered in the design of the trace width of the RF transmission line.
☐	Whether the entire matching network has been as close to the chip as possible.
☐	Whether try not to have silk screen on RF devices and traces.
☐	Whether the RF trace and the ground plane around it are flat.
☐	Whether the length of the monopole antenna is close to λ/4.
☐	Whether the width of the PCB antenna exceeds 1 mm.
Crystal Circuit Design	
☐	Whether the crystal has been as close to the xtal pin as possible.
☐	Whether the crystal has been as far away from the PA output, antenna, and digital tracing as possible, and whether ground plane as much as possible has been placed around the crystal for isolation.
☐	Whether the metal casing of the crystal is grounded.
Digital Signal Design	
☐	Whether the digital signal has been as far away from the crystal and RF trace as possible.
☐	Whether has tried to place ground plane all around the digital signal.
Ground Design	
☐	Whether has tried to place continuous ground plane as large as possible.
☐	Whether the ground trace has made the current loop as short as possible.
☐	Whether has placed vias as many as possible with a size no more than λ/10 on PCB edges.

7. Revise History

Table 6. Revise History Records

Version No.	Chapter	Description	Date
0.8	All	Initial version.	2017-09-12
0.9	2.2	Add capacitors C5,C6 and resistor R1.	2020-08-06

8. Contacts

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