CMOSTEK

AN236

CMT2310A Register Description

Overview

This application document provides register introduction for users who use CMT2310A for product development, so that users can refer to the description and usage of each register during processing.

The product models covered in this document are shown in the table below.

Table 1. Product Models Covered in this Document

Part Number	Frequency	Modem	Function	Configuration	Package
CMT2310A	113 - 960 MHz	(4)(G)FSK/OOK	Transceiver	Register	QFN24

Users should jointly read the documents below to get comprehensive information on software and hardware development.

AN238 CMT2310A RF Parameter Configuration Guide

AN235 CMT2310A FIFO and Packet Format Usage Guide

AN237 CMT2310A Quick Start Guide

AN239 CMT2310A Automatic Receiving and Transmission Function Usage Guide

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1 Register Introduction

1.1 PAGE 0, Control Register（0x00 - 0x27）

Registers in this area are mainly to control the switching of chip operating mode and interrupt related operating.

Table 2. PAGE 0 (0x00 - 0x27), Control Register Description

Register Name	Bits	R/W	Bit Flag	Description
CTL_REG_0 (0x00)	7:0	W	PU_BOOT <7:0>	The register sends out 0x03 to power on the chip in IDLE state and then make the chip to stay in SLEEP state. It is not allowed to set other values
CTL_REG_1 (0x01)	7:0	W	CHIP_MODE_SW<7:0>	Chip state switching command 00000001：go_sleep 00000010：go_ready 00000100：go_tx 00001000：go_rx 00010000：go_tfs 00100000：go_rfs Except for the 6 values above, others are invalid.
CTL_REG_2 (0x02)	7:2	RW	RESV	Reserve bit，it has to set all 0
	1	RW	ANT_DIV_MANU	Antenna diversity manual mode enables： 0：disable 1：enable
	0	RW	ANT_SELECT	Antenna selected in antenna diversity manual mode： 0：antenna 1 1：antenna 2
CTL_REG_3 (0x03)	7:0	RW	FREQ_CHANL_MANU<7:0>	Manually set the channel value in fast frequency hopping mode
CTL_REG_4 (0x04)	7	RW	RESV	Reserve bit，it is set to 0
	6	RW	TX_DIN_EN	0: disable Tx data to be input from GPIO 1: enable Tx data to be input from GPIO
	5:3	RW	GPIO1_SEL<2:0>	Select GPIO1 function. 000: DCLK 001: INT1 010: INT2 011: DOUT Other selections: NA

Register Name	Bits	R/W	Bit Flag	Description
	2:0	RW	GPIO0_SEL<2:0>	Select GPIO1 function： 000：DOUT 001：INT1 010：INT2 011：DCLK 110：INT3 Other selections：NA
CTL_REG_5 (0x05)	7:6	RW	TX_DIN_SEL<1:0>	Select which GPIO to input the transmitting data: 00：GPIO3 01：GPIO4 10：NIRQ 11：NA
	5:3	RW	GPIO3_SEL<2:0>	Select the GPIO3 function： 000：INT2 001：INT1 010：DCLK 011：DOUT 101：DIN Other selections：NA
	2:0	RW	GPIO2_SEL<2:0>	Select the GPIO2 function. 000：INT1 001：INT2 010：DCLK 011：DOUT 110：INT3 Other selections：NA
CTL_REG_6 (0x06)	7	RW	RESV	Reserve bit，it has to be set as 0
	6	RW	DIG_CLKOUT_EN	Set GPIO4 as digital clock output. 0: disable 1: enable The item has higher priority than other GPIO4 configurations.
	5:3	RW	GPIO5_SEL<2:0>	Select GPIO5 function. 000: RSTn 001: INT1 010: INT2 011: DOUT 100: DCLK Other options: NA
	2:0	RW	GPIO4_SEL<2:0>	Select GPIO4 function.

Register Name	Bits	R/W	Bit Flag	Description
				000: DOUT 001: INT1 010: INT2 011: DCLK 101: DIN Other options: NA
CTL_REG_7 (0x07)	7:6	RW	RESV	Reserve bit，it has to be set as 00
	5	RW	LFXO_PAD_EN	Set GPIO2 and GPIO3 as the two pins of LFXO. 0: disable. 1: enable. The item has higher priority than other GPIO2 and GPIO3 configurations.
	4	RW	API_STOP	Stop the API that the chip is executing. 0：API in progress 1：API stop
	3	RW	SPI_3W_EN	Switch the chip SPI interface to 3-wire mode. 0: 4-wire mode. 1: 3-wire mode.
	2:0	RW	NIRQ_SEL<2:0>	Select NIRQ function. 000：INT1 001：INT2 010：DCLK 011：DOUT 100：TCXO 101：DIN Other options: NA
CTL_REG_8 (0x08)	6:0	W	API_CMD<6:0>	API command input interface.
CTL_REG_9 (0x09)	7	R	API_CMD_FLAG	API command flag
	6:0	R	API_RESP<6:0>	Feedback or response of API command execution.
CTL_REG_10 (0x0A)	7:0	R	CHIP_MODE_STA<7:0>	Current state of the chip. 00000000：IDLE 10000001：SLEEP 10000010：READY 10000100：RFS 10001000：TFS 10010000：RX 10100000：TX IDLE indicates that no operation is

Register Name	Bits	R/W	Bit Flag	Description
				performed after the chip is powered on.Other values are invalid.
CTL_REG_11 (0x0B)	7:0	R	FREQ_DONE_TIMES<7:0>	Automatic frequency hopping completion times are valid from 0 to 63
CTL_REG_12 (0x0C)	7:0	RW	FREQ_SPACE<7:0>	Channel interval for automatic frequency hopping.
CTL_REG_13 (0x0D)	7:0	RW	FREQ_TIMES<7:0>	Automatic frequency hopping times are valid from 1 to 64
CTL_REG_14 (0x0E)	7	RW	RX_FIFO_FULL_EN	RX FIFO full interruption enabled. 0：disable 1：enable
	6	RW	RX_FIFO_NMTY_EN	RX FIFO not empty interruption enabled. 0：disable 1：enable
	5	RW	RX_FIFO_TH_EN	RX FIFO unread content exceed the FIFO TH interruption enabled. 0：disable 1：enable
	4	RW	RESV	Reserve bit，it is set as 0
	3	RW	RX_FIFO_OVF_EN	RX FIFO overflow interruption enabled. 0：disable 1：enable
	2	RW	TX_FIFO_FULL_EN	TX FIFO full interruption enabled. 0：disable 1：enable
	1	RW	TX_FIFO_NMTY_EN	TX FIFO not empty interruption enabled. 0：disable 1：enable
	0	RW	TX_FIFO_TH_EN	TX FIFO unread content exceed the FIFO TH interruption enabled. 0：disable 1：enable
CTL_REG_15 (0x0F)	7:1	R	RESV	Reserve bit, cannot write, read value can be ignored.
	0	R	ANT_INSTR	Instruct the locking antenna of the antenna diversity.
CTL_REG_16 (0x10)	7:6	RW	RESV	Reserve bit，it has to be set as 0
	5:0	RW	INT1_SEL<5:0>	Selection of interruption source when INT1 is mode 1. 000000：INT_MIX，all interruption combination

Register Name	Bits	R/W	Bit Flag	Description
				000001：ANT_LOCK 000010：RSSI_PJD_VALID 000011：PREAM_PASS 000100：SYNC_PASS 000101：ADDR_PASS 000110：CRC_PASS 000111：PKT_OK 001000：PKT_DONE 001001：SLEEP_TMO 001010：RX_TMO 001011：RX_FIFO_NMTY 001100：RX_FIFO_TH 001101：RX_FIFO_FULL 001110：RX_FIFO_WBYTE 001111：RX_FIFO_OVF 010000：TX_DONE 010001：TX_FIFO_NMTY 010010：TX_FIFO_TH 010011：TX_FIFO_FULL 010100：STATE_IS_READY 010101：STATE_IS_FS 010110：STATE_IS_RX 010111：STATE_IS_TX 011000：LBD_STATUS 011001：API_CMD_FAILED 011010：API_DONE 011011：TX_DC_DONE 011100：ACK_RECV_FAILED 011101：TX_RESEND_DONE 011110：NACK_RECV 011111：SEQ_MATCH 100000：CSMA_DONE 100001：CCA_STATUS
CTL_REG_17 (0x11)	7	RW	INT1_POLAR	The polarity of interrupt 1： 0: high active. 1: low active.
	6	RW	INT2_POLAR	The polarity of interrupt 2： 0: high active. 1: low active.
	5:0	RW	INT2_SEL<5:0>	Selection of interruption source when INT2 is mode 1.

Register Name	Bits	R/W	Bit Flag	Description
				000000：INT_MIX，all interruption combination 000001：ANT_LOCK 000010：RSSI_PJD_VALID 000011：PREAM_PASS 000100：SYNC_PASS 000101：ADDR_PASS 000110：CRC_PASS 000111：PKT_OK 001000：PKT_DONE 001001：SLEEP_TMO 001010：RX_TMO 001011：RX_FIFO_NMTY 001100：RX_FIFO_TH 001101：RX_FIFO_FULL 001110：RX_FIFO_WBYTE 001111：RX_FIFO_OVF 010000：TX_DONE 010001：TX_FIFO_NMTY 010010：TX_FIFO_TH 010011：TX_FIFO_FULL 010100：STATE_IS_READY 010101：STATE_IS_FS 010110：STATE_IS_RX 010111：STATE_IS_TX 011000：LBD_STATUS 011001：API_CMD_FAILED 011010：API_DONE 011011：TX_DC_DONE 011100：ACK_RECV_FAILED 011101：TX_RESEND_DONE 011110：NACK_RECV 011111：SEQ_MATCH 100000：CSMA_DONE 100001：CCA_STATUS
CTL_REG_18 (0x12)	7	RW	SLEEP_TMO_EN	0：disable SLEEP_TMO interruption 1：enable SLEEP_TMO interruption
	6	RW	RX_TMO_EN	0：disable RX_TMO interruption 1：enable RX_TMO interruption
	5	RW	TX_DONE_EN	0：disable TX_DONE interruption 1：enable TX_DONE interruption

Register Name	Bits	R/W	Bit Flag	Description
	4	RW	PREAM_PASS_EN	0：disable PREAM_PASS interruption 1：enable PREAM_PASS interruption
	3	RW	SYNC_PASS_EN	0：disable SYNC_PASS interruption 1：enable SYNC_PASS interruption
	2	RW	ADDR_PASS_EN	0：disable ADDR_PASS interruption 1：enable ADDR_PASS interruption
	1	RW	CRC_PASS_EN	0：disable CRC_PASS interruption 1：enable CRC_PASS interruption
	0	RW	PKT_DONE_EN	0：disable PKT_DONE interruption 1：enable PKT_DONE interruption
CTL_REG_19 (0x13)	7	RW	INT3_POLAR	The polarity of interrupt 3： 0：high effective 1：low effective
	6	RW	PD_FIFO	0：Save the FIFO content in the SLEEP state 1：The FIFO content is not saved in the SLEEP state
	5	RW	FIFO_TH<8>	The 8th bit of FIFO_TH.
	4	RW	FIFO_AUTO_CLR_RX_EN	Automatically clear RX FIFO content before configuring into RX. 0：not clear 1：clear
	3	RW	FIFO_AUTO_RES_TX_EN	Restore TX FIFO automatically after each packet transmission. If it requires to send more than 1 packet repeatedly (TX_PKT_NUM> 0), this bit must be set as 1.
	2	RW	FIFO_TX_TEST_EN	0：TX FIFO can only be written through SPI 1: SPI supports Read operation on TX FIFO. This bit is only valid to TX FIFO. It should always be set as 0 except for user testing usage.
	1	RW	FIFO_MERGE_EN	0: separate as 2 128-byte FIFOs. 1: merge into 1 256-byte FIFO.
	0	RW	FIFO_TX_RX_SEL	When FIFO under merged mode， 0：FIFO can be used as TX FIFO 1：FIFO can be used as RX FIFO
CTL_REG_20 (0x14)	7:0	RW	FIFO_TH<7:0>	The FIFO filling threshold unit is byte. For RX, when the unread data exceed the threshold, RX_FIFO_TH_FLG is set to 1; for TX, when the unsent data is under the threshold, TX_FIFO_TH_FLG is set to 0.

Register Name	Bits	R/W	Bit Flag	Description
				When FIFO_MERGE_EN = 0, the valid range is 1 - 127.; When FIFO_MERGE_EN = 1, the valid range is 1 - 255.
CTL_REG_21 (0x15)	7	RW	RESV	Reserve bit, it has to be set as 0.
	6	RW	RSSI_PJD_VALID_EN	0：disable RSSI_PJD_VALID interruption 1：enable RSSI_PJD_VALID interruption
	5	RW	OP_CMD_FAILED_EN	0：disable API_CMD_FAILED interruption 1：enable API_CMD_FAILED interruption
	4	RW	RSSI_COLL_EN	0：disable RSSI_COLL interruption 1：enable RSSI_COLL interruption
	3	RW	PKT_ERR_EN	0：disable PKT_ERR interruption 1：enable PKT_ERR interruption
	2	RW	LBD_STATUS_EN	0：disable LBD_STATUS interruption 1：enable LBD_STATUS interruption
	1	RW	LBD_STOP_EN	0：disable LBD_STOP interruption 1：enable LBD_STOP interruption
	0	RW	LD_STOP_EN	0：disable LD_STOP interruption 1：enable LD_STOP interruption
CTL_REG_22 (0x16)	7	RW	FREQ_HOP_MANU_EN	0：disable manually fast frequency sweep 1：enable manually fast frequency sweep
	6	RW	RX_HOP_PERSIST	RX automatically frequency hopping setting： 0：complete the setting times 1：keep going
	5	RW	FREQ_SW_STATE	In the case of RX frequency hopping, users can select to back to a certain state and return back to RX state to continue receiving the next channel when it is overtime. 0：back to READY state 1：back to RFS state
	4	RW	TX_DATA_INV	0：not reverse the transmission data input from GPIO. 1：reverse the transmission data input from GPIO.
	3	RW	RESV	Reserve bit, it has to be set as 0.
	2	RW	TRX_SWT_INV	Control the two output values of the TX/RX antenna switch: 0：not reverse 1：reverse

Register Name	Bits	R/W	Bit Flag	Description
	1	RW	TRX_SWT_EN	Set the GPIO 0 and GPIO 1 as the control output of TX / RX antenna switch. It has higher priority than the GPIO0_SEL and GPIO1_SEL.
	0	RW	ANT_LOCK_EN	0：disable ANT_LOCK interruption 1：enable ANT_LOCK interruption
CTL_REG_23 (0x17)	7	RW	API_DONE_EN	0：disable API_DONE interruption 1：enable API_DONE interruption
	6	RW	CCA_STATUS_EN	0：disable CCA_STATUS interruption 1：enable CCA_STATUS interruption
	5	RW	CSMA_DONE_EN	0：disable CSMA_DONE interruption 1：enable CSMA_DONE interruption
	4	RW	TX_DC_DONE_EN	0：disable TX_DC_DONE interruption 1：enable TX_DC_DONE interruption
	3	RW	ACK_RECV_FAILED_EN	0：disable ACK_RECV_FAILED interruption 1：enable ACK_RECV_FAILED interruption
	2	RW	TX_RESEND_DONE_EN	0：disable TX_RESEND_DONE interruption 1：enable TX_RESEND_DONE interruption
	1	RW	NACK_RECV_EN	0：disable NACK_RECV interruption 1：enable NACK_RECV interruption
	0	RW	SEQ_MATCH_EN	0：disable SEQ_MATCH interruption 1：enable SEQ_MATCH interruption
CTL_REG_24 (0x18)	7:6	R	RESV	Reserve bit, it is set as 0.
	5	R	SLEEP_TMO_FLG	SLEEP_TMO interruption flag
	4	R	RX_TMO_FLG	RX_TMO interruption flag
	3	R	TX_DONE_FLG	TX_DONE interruption flag
	2	W	SLEEP_TMO_CLR	SLEEP_TMO interruption clear 0：no action 1：clear
	1	W	RX_TMO_CLR	RX_TMO interruption clear 0：no action 1：clear
	0	W	TX_DONE_CLR	TX_DONE interruption clear 0：no action 1：clear
CTL_REG_25 (0x19)	7:5	W	RESV	Reserve bit, it has to be set as 0.
	4	W	PREAM_PASS_CLR	PREAM_PASS interruption clear 0：no action 1：clear

Register Name	Bits	R/W	Bit Flag	Description
	3	W	SYNC_PASS_CLR	SYNC_PASS interruption clear 0：no action 1：clear
	2	W	ADDR_PASS_CLR	ADDR_PASS interruption clear 0：no action 1：clear
	1	W	CRC_PASS_CLR	CRC_PASS interruption clear 0：no action 1：clear
	0	W	PKT_DONE_CLR	PKT_DONE interruption clear 0：no action 1：clear
CTL_REG_26 (0x1A)	7:6	R	RESV	Reserve bit, read value can be ignored
	5	R	SYNC1_PASS_FLG	SYNC1_PASS interruption flag
	4	R	PREAM_PASS_FLG	PREAM_PASS interruption flag
	3	R	SYNC_PASS_FLG	SYNC_PASS interruption flag
	2	R	ADDR_PASS_FLG	ADDR_PASS interruption flag
	1	R	CRC_PASS_FLG	CRC_PASS interruption flag
	0	R	PKT_DONE_FLG	PKT_DONE interruption flag
CTL_REG_27 (0x1B)	7:3	W	RESV	Reserve bit, it has to be set as 0.
	2	W	TX_FIFO_RESTORE	Provides manually restore TX FIFO function. Restore means reset red pointer and keep the write pointer unchanged, which makes TX FIFO back to unread state and resend the already filled in data.
	1	W	RX_FIFO_CLR	0：invalid，1：clear RX FIFO Users don't need to set it back to 0 when the bit is 1 since it will back to 0 internally.
	0	W	TX_FIFO_CLR	0：invalid，1：clear TX FIFO Users don't need to set it back to 0 when the bit is 1 since it will back to 0 internally.
CTL_REG_28 (0x1C)	7	R	RX_FIFO_FULL_FLG	Interruption flag of RX FIFO full 0：invalid 1：valid
	6	R	RX_FIFO_NMTY_FLG	Interruption flag of RX FIFO not empty 0：invalid 1：valid
	5	R	RX_FIFO_TH_FLG	Interruption indicates that RX FIFO unread content exceeds FIFO TH 0：invalid 1：valid

Register Name	Bits	R/W	Bit Flag	Description
	4	R	RESV	Reserved bit. The read value can be ignored
	3	R	RX_FIFO_OVF_FLG	Interruption indicates RX FIFO overflow 0：invalid 1：valid
	2	R	TX_FIFO_FULL_FLG	Interruption indicates TX FIFO full 0：invalid 1：valid
	1	R	TX_FIFO_NMTY_FLG	Interruption indicates TX FIFO not empty 0：invalid 1：valid
	0	R	TX_FIFO_TH_FLG	Interruption indicates that TX FIFO unread content exceeds FIFO TH 0：invalid 1：valid
CTL_REG_29 (0x1D)	7:5	W	RESV	Reserve bit, it has to be set as 0.
	4	W	ANT_LOCK_CLR	ANT_LOCK interruption clear 0：no action 1：clear
	3	W	OP_CMD_FAILED_CLR	OP_CMD_FAILED interruption clear 0：no action 1：clear
	2	W	RSSI_COLL_CLR	RSSI_COLL interruption clear 0：no action 1：clear
	1	W	PKT_ERR_CLR	PKT_ERR interruption clear 0：no action 1：clear
	0	W	LBD_STATUS_CLR	LBD_STATUS interruption clear 0：no action 1：clear
CTL_REG_30 (0x1E)	7:5	R	RESV	Reserve bit, read data can be ignored.
	4	R	ANT_LOCK_FLAG	ANT_LOCK interruption flag
	3	R	OP_CMD_FAILED_FLG	OP_CMD_FAILED interruption flag
	2	R	RSSI_COLL_FLG	RSSI_COLL interruption flag
	1	R	PKT_ERR_FLG	PKT_ERR interruption flag
	0	R	LBD_STATUS_FLG	LBD_STATUS interruption flag
CTL_REG_31 (0x1F)	7	W	API_DONE_CLR	API_DONE interruption clear 0：no action 1：clear
	6	W	CCA_STATUS_CLR	CCA_STATUS interruption clear

Register Name	Bits	R/W	Bit Flag	Description
				0：no action 1：clear
	5	W	CSMA_DONE_CLR	CSMA_DONE interruption clear 0：no action 1：clear
	4	W	TX_DC_DONE_CLR	TX_DC_DONE interruption clear 0：no action 1：clear
	3	W	ACK_RECV_FAILED_CLR	ACK_RECV_FAILED interruption clear 0：no action 1：clear
	2	W	TX_RESEND_DONE_CLR	TX_RESEND_DONE interruption clear 0：no action 1：clear
	1	W	NACK_RECV_CLR	NACK_RECV interruption clear 0：no action 1：clear
	0	W	SEQ_MATCH_CLR	SEQ_MATCH interruption clear 0：no action 1：clear
CTL_REG_32 (0x20)	7	R	API_DONE_FLG	API_DONE interruption flag
	6	R	CCA_STATUS_FLG	CCA_STATUS interruption flag
	5	R	CSMA_DONE_FLG	CSMA_DONE interruption flag
	4	R	TX_DC_DONE_FLG	TX_DC_DONE interruption flag
	3	R	ACK_RECV_FAILED_FLG	ACK_RECV_FAILED interruption flag
	2	R	TX_RESEND_DONE_FLG	TX_RESEND_DONE interruption flag
	1	R	NACK_RECV_FLG	NACK_RECV interruption flag
	0	R	SEQ_MATCH_FLG	SEQ_MATCH interruption flag
CTL_REG_33 (0x21)	1:0	R	RSSI_VALUE_MIN<7:0>	In the case of antenna diversity, the RSSI read value of the antenna with the lower receiving signal strength is obtained among the two antennas,
CTL_REG_34 (0x22)	7:0	R	RSSI_VALUE<7:0>	The RSSI read value，with a unit of dbm
CTL_REG_35 (0x23)	7:0	R	LBD_DATA<7:0>	Low battery detection. value
CTL_REG_36 (0x24)	7:0	R	TEMP_DATA<7:0>	Temperature detection value
CTL_REG_37 (0x25)	7:0	R	FREQ_CHANL_ACT<7:0>	The current used channel value under automatic frequency hopping.
CTL_REG_38	7:0	R	SEQNUM_TX_OUT<7:0>	Currently TX sequence value.

Register Name	Bits	R/W	Bit Flag	Description
(0x26)				
CTL_REG_39 (0x27)	7:0	R	SEQNUM_TX_OUT<15:8>	

1.2 PAGE 0, Configuration Register（0x28 - 0x77）

Registers in this area is used for configurations of packet format, FIFO, and system operating mechanism.

Table 3. PAGE 0 (0x28 - 0x77), Configuration Register Description

Register Name	Bits	R/W	Bit Flag	Description
CTL_REG_40 (0x28)	7:3	RW	RX_PREAM_SIZE<4:0>	Preamble length in RX mode with a range of 0 -31 length units. 0 represents it does not detect Preamble; 1 represents it detects Preamble with 1 length unit, and so on.
	2	RW	PREAM_LENG_UNIT	The length unit of Preamble is shared by TX and RX.： 0：the length unit is 8 bits 1：the length unit is 4 bits
	1:0	RW	DATA_MODE<1:0>	Select data mode for transmitting and receiving data. 0：Direct mode（default） 1：NA 2：Packet mode 3：NA
CTL_REG_41 (0x29)	7:0	RW	TX_PREAM_SIZE<7:0>	The Preamble length in TX mode can be configured with a range of 0 - 65535 length units. 0 represents it does not send out Preamble; 1 represents it sends out Preamble with 1 length unit, and so on.
CTL_REG_42 (0x2A)	7:0	RW	TX_PREAM_SIZE<15:8>	
CTL_REG_43 (0x2B)	7:0	RW	PREAM_VALUE<7:0>	The Preamble value is shared by both TX and RX： When PREAM_LEN_UNIT = 0, all the 8 bits are valid. When PREAM_LEN_UNIT = 1, only bits <3:0> is valid.
CTL_REG_44 (0x2C)	7	RW	SYNC_MODE_SEL	Sync detection mode： 0：normal mode 1：compatible with 802.15.4 mode
	6:4	RW	SYNC_TOL<2:0>	Number of error-tolerant bits for Sync Word detection in RX mode： 0: not allowed for error 1: allowed for error receiving of 1bit 2: allowed for error receiving of 2bits 3: allowed for error receiving of 3bits 4: allowed for error receiving of 4bits

Register Name	Bits	R/W	Bit Flag	Description
				5: allowed for error receiving of 5bits 6: allowed for error receiving of 6bits 7: allowed for error receiving of 7bits
	3:1	RW	SYNC_SIZE<2:0>	Sync Word length： 0: 1 byte 1: 2 bytes 2: 3 bytes 3: 4 bytes 4: 5 bytes 5: 6 bytes 6: 7 bytes 7: 8 bytes
	0	RW	SYNC_MAN_EN	The enabling Manchester Codec of Sync Word 0：disable 1：enable
CTL_REG_45 (0x2D)	7:0	RW	SYNC_VALUE<7:0>	Sync Word values are filled into different registers according to the SYNC_SIZE Settings, more details please refer to the following table.
CTL_REG_46 (0x2E)	7:0	RW	SYNC_VALUE<15:8>	
CTL_REG_47 (0x2F)	7:0	RW	SYNC_VALUE<23:16>	
CTL_REG_48 (0x30)	7:0	RW	SYNC_VALUE<31:24>	
CTL_REG_49 (0x31)	7:0	RW	SYNC_VALUE<39:32>	
CTL_REG_50 (0x32)	7:0	RW	SYNC_VALUE<47:40>	
CTL_REG_51 (0x33)	7:0	RW	SYNC_VALUE<55:48>	
CTL_REG_52 (0x34)	7:0	RW	SYNC_VALUE<63:56>	
CTL_REG_53 (0x35)	7:0	RW	SYNC_FEC_VALUE<7:0>	The value of Sync_fec is filled into different registers according to the SYNC_SIZE setting, more details please refer to the following table.
CTL_REG_54 (0x36)	7:0	RW	SYNC_ FEC_VALUE<15:8>	
CTL_REG_55 (0x37)	7:0	RW	SYNC_ FEC_VALUE<23:16>	
CTL_REG_56 (0x38)	7:0	RW	SYNC_ FEC_VALUE<31:24>	
CTL_REG_57 (0x39)	7:0	RW	SYNC_ FEC_VALUE<39:32>	

Register Name	Bits	R/W	Bit Flag	Description
CTL_REG_58 (0x3A)	7:0	RW	SYNC_ FEC_VALUE<47:40>	
CTL_REG_59 (0x3B)	7:0	RW	SYNC_ FEC_VALUE<55:48>	
CTL_REG_60 (0x3C)	7:0	RW	SYNC_ FEC_VALUE<63:56>	
CTL_REG_61 (0x3D)	7:0	RW	PAYLOAD_LENGTH<7:0>	The length of the content excluding PREAMBLE and SYNC in the packet format. Payload = length (optional) + address (optional) + fcs1 (optional) + fcs2 (optional) + data. Both of the destination and data source are FIFO. This configuration is applicable to both packets with fixed length and variable length.
CTL_REG_62 (0x3E)	7:0	RW	PAYLOAD_LENGTH<15:8>	
CTL_REG_63 (0x3F)	7	RW	INTERLEAVE_EN	The enabling of interleaving function. 0: disable. 1: enable.
	6	RW	RESV	Reserved bit，it has to be set as 0
	5	RW	LENGTH_SIZE	Length selection of the variable length packet： 0: 1 byte, supporting variable packet length up to 255 bytes. 1: 2 bytes, supporting variable packet length up to 65535 bytes.
	4	RW	PAGGYBACKING_EN	Whether the automatic reply packet carries payload： 0：not carry payload 1：carry payload
	2	RW	ADDR_LEN_CONF	The positions of Node ID and Length Byte in variable-length packet. 0：Node ID is before length Byte. 1：Node ID is after length Byte.
	1	RW	PAYLOAD_BIT_ORDER	0: encoding each byte MSB of payload+CRC first 1: encoding each byte LSB of payload+CRC first
	0	RW	PKT_TYPE	Packet length type 0: fixed packet length 1: variable packet length
CTL_REG_64 (0x40)	7	RW	SYNC_VALUE_SEL	It's valid when SYNC_MODE_SEL is 0. 0: select SYNC_VALUE. 1: select SYNC_FEC_VALUE.
	6	RW	ADDR_SPLIT_MODE	The configuration of splitting address. 0：Only DEST ADDR, that is, NODE_ADDR is used to configure DEST ADDR only. 1: DEST ADDR + SRC ADDR, that is, the higher 16 bits of NODE_ADDR are used to configure DEST ADDR and

Register Name	Bits	R/W	Bit Flag	Description
				the lower 16 bits are used to configure SRC ADDR.
	5	RW	ADDR_FREE_EN	The enabling bit to separate ADDR detection circuit in RX mode. 0: disable. 1: enable.
	4	RW	ADDR_ERR_MASK	Upon ADDR detection error, it will output the PKT_ERR interrupt and synchronously reset decoder circuit. This bit controls whether to reset the circuit at the same time. 0: reset synchronously 1: not reset synchronously
	3:2	RW	ADDR_SIZE<1:0>	The length of ADDR. 0: 1 byte 1: 2 bytes 2: 3 bytes 3: 4 bytes When ADDR_SPLIT_MODE is 1, it represents that DEST ADDR and SRC ADDR occupy 1~2 bytes respectively.
	1:0	RW	ADDR_ DET_MODE <1:0>	The detection mode of ADDR. 0: not detect. 1: it transmits the content of ADDR_VALUE in TX mode and identifies the content of ADDR_VALUE in RX mode. 2: it transmits the content of ADDR_VALUE in TX mode; and identifies both the content of ADDR_VALUE and the content all 0 in RX mode. 3: it transmits the content of ADDR_VALUE in TX mode; it identifies both the content of ADDR_VALUE and the content of all 0 or all 1 in RX mode.
CTL_REG_65 (0x41)	7:0	RW	SRC_ADDR<7:0>	ADDR value of the local source device, it can be configured 1 to 2 bytes.
CTL_REG_66 (0x42)	7:0	RW	SRC_ADDR<15:8>	
CTL_REG_67 (0x41)	7:0	RW	DEST_ADDR<7:0>	ADDR value of the destination device, it can be configured 1 to 2 bytes.
CTL_REG_68 (0x42)	7:0	RW	DEST_ADDR<15:8>	
CTL_REG_69 (0x45)	7:0	RW	SRC_BITMASK<7:0>	The bit mask decides whether to compare each receiving bit of the corresponding SRC_ADDR. 0：allowed to compare 1：not compare
CTL_REG_70 (0x46)	7:0	RW	SRC_BITMASK<15:8>	
CTL_REG_71	7:0	RW	DEST_BITMASK<7:0>	The bit mask decides whether to compare each

Register Name	Bits	R/W	Bit Flag	Description
(0x47)				receiving bit of the corresponding DEST_ADDR. 0：allowed to compare 1：not compare
CTL_REG_72 (0x48)	7:0	RW	DEST_BITMASK<15:8>	
CTL_REG_73 (0x49)	7:6	RW	CRC_SIZE<1:0>	Byte number of the CRC verification code 0: 1 byte. 1: 2 bytes. 2: 3 bytes. 3: 4 bytes.
	5	RW	CRC_BYTE_SWAP	Receiving/sending sequence of CRC 0: sending/receiving higher byte first. 1: sending/receiving lower byte first.
	4	RW	CRC_BIT_INV	Whether to reverse CRC code. 0: not reverse CRC code. 1: reverse CRC code bit by bit.
	3	RW	CRC_RANGE	The CRC calculation range. 0: the entire payload. 1: data only.
	2	RW	CRC_REFIN	The bit sequence reverse of the input byte in CRC calculation.
	1	RW	CRC_BIT_ORDER	Receiving/sending bit sequence of CRC 0: sending/receiving higher byte first. 1: sending/receiving lower byte first.
	0	RW	CRC_EN	CRC enabling. 0: disable. 1: enable.
CTL_REG_74 (0x4A)	7:0	RW	CRC_SEED<7:0>	The initial value of the polynomial for CRC.
CTL_REG_75 (0x4B)	7:0	RW	CRC_SEED<15:8>	
CTL_REG_76 (0x4C)	7:0	RW	CRC_SEED<23:16>	
CTL_REG_77 (0x4D)	7:0	RW	CRC_SEED<31:24>	
CTL_REG_78 (0x4E)	7:0	RW	CRC_POLY<7:0>	The polynomial for CRC calculation.
CTL_REG_79 (0x4F)	7:0	RW	CRC_POLY <15:8>	
CTL_REG_80 (0x50)	7:0	RW	CRC_POLY <23:16>	
CTL_REG_81 (0x51)	7:0	RW	CRC_POLY <31:24>	

Register Name	Bits	R/W	Bit Flag	Description
CTL_REG_82 (0x52)	7	RW	CRC_REFOUT	Reverse sequence of all the output bytes in CRC calculation 0：From MSB to LSB； 1：From LSB to MSB.
	6	RW	WHITEN_SEED<8>	The highest bit of WHITEN_SEED.
	5	RW	WHITEN_SEED_TYPE	The seed type under PN7 whitening codec polynomial. 0：PN7 seed is calculated according to A7139 1：PN7 seed is the valued defined in whiten_seed.
	4:3	RW	WHITEN_TYPE<1:0>	The method of whitening encoding/decoding. 0: PN9 CCITT encoding/decoding 1: PN9 IBM encoding/decoding 2: PN7 encoding/decoding 3: invalid
	2	RW	WHITEN_EN	The enabling of whitening encoding/decoding. 0: disable. 1: enable.
	1	RW	MANCH_TYPE	The way of Manchester encoding/decoding. 0: 01 represents 1 and 10 represents 0. 1: 10 represents 1 and 01 represents 0.
	0	RW	MANCH_EN	The enabling of Manchester encoding/decoding. 0: disable. 1: enable.
CTL_REG_83 (0x53)	7:0	RW	WHITEN_SEED<7:0>	The seed for the polynomial of the whitening encoding/decoding. If it is PN9, it takes all 9 bit If it is PN7, it takes lower 7bit
CTL_REG_84 (0x54)	7	RW	CRCERR_CLR_FIFO_EN	Mismatch happens at CRC receiving 0：not clear RX FIFO 1：clear RX FIFO
	6	RW	FCS2_EN	Whether to contain FCS2 0：with no FCS2 1：with FCS2
	5	RW	SEQNUM_MATCH_EN	Whether to compare the receiving sequence number with the local transmitting sequence number at the TX terminal under TX ack. 0：no need to compare 1：need to compare
	4	RW	SEQNUM_SIZE	The size of SEQNUM. 0: 1 byte. 1: 2 bytes.

Register Name	Bits	R/W	Bit Flag	Description
	3	RW	SEQNUM_AUTO_INC	Whether the TX SEQNUM increase automatically 0：not increase 1: increase by 1 automatically for each packet.
	2	RW	SEQNUM_EN	0: disable SEQNUM field (namely FCS1) 1: enable SEQNUM field (namely FCS1)
	1:0	RW	RESV	Reserve bit and it has to write as 0.
CTL_REG_85 (0x55)	7:0	RW	TX_PKT_NUM<7:0>	The repeatedly send out packet number under TX mode each time: 0-65535 represents sending out 1-65536 packets.
CTL_REG_86 (0x56)	7:0	RW	TX_PKT_NUM<15:8>	
CTL_REG_87 (0x57)	7:0	RW	SEQNUM_TX_IN<7:0>	The initializing value of TX SEQNUM.
CTL_REG_88 (0x58)	7:0	RW	SEQNUM_TX_IN<15:8>	
CTL_REG_89 (0x59)	7:0	RW	TX_PKT_GAP<7:0>	The interval between packets when transmitting packets repeatedly under TX mode 0-255 represents for 1-256 Symbol interval between packets.
CTL_REG_90 (0x5A)	7:0	RW	RSSI_CAL_OFFSET<7:0>	It is used for manually offset the deviation of RSSI reading value, which is filled after actual measurement.
CTL_REG_91 (0x5B)	7:0	RW	FCS2_TX_IN<7:0>	The transmitting value of FCS2 at TX side.
CTL_REG_92 (0x5C)	7:0	RW	FCS2_RX_OUT<7:0>	Output the received FCS2 value into the register in FCS2 enabling.
CTL_REG_93 (0x5D)	7	RW	FEC_TICC	Polynomial selection of the NRNSC： 0：In FEC polynomial structure, u_i takes reverse output 1：In FEC polynomial structure, u_i doesn't take reverse output
	6:2	RW	FEC_PAD_CODE<12:8>	The padding code of FEC is configured higher5 bits.
	1	RW	FEC_RSC_NRNSC_SEL	Whether FEC selects RSC or NRNSC. 0: RSC. 1: NRNSC.
	0	RW	FEC_EN	The enabling bit of FEC. 0: disable FEC encoding/decoding. 1: enable FEC encoding/decoding.
CTL_REG_94 (0x5E)	7:0	RW	FEC_PAD_CODE<7:0>	The padding code of FEC is configured lower 8 bits.
CTL_REG_95	7:6	RW	MAP_4FSK_3_LEVEL<1:0>	The code value that represents the highest level in

Register Name	Bits	R/W	Bit Flag	Description
(0x5F)				4FSK in RX mode.
	5:4	RW	MAP_4FSK_2_LEVEL<1:0>	The code value that represents the second highest level in 4FSK in RX mode.
	3:2	RW	MAP_4FSK_1_LEVEL<1:0>	The code value that represents the third highest level in 4FSK in RX mode.
	1:0	RW	MAP_4FSK_0_LEVEL<1:0>	The code value that represents the fourth highest level in 4FSK in RX mode.
CTL_REG_96 (0x60)	7	RW	RESV	Reserve bit and it has to write as 0.
	6:4	RW	TX_EXIT_STATE<2:0>	Exiting the setting status automatically once it completes the transmission. 1：SLEEP 2：READY 3：TFS 4：TX 5：RFS 6：RX Others：SLEEP The chip only exits TX automatically after transmission completes under packet mode, otherwise it will wait until the MCU sends the go_* command to switch.
	3	RW	TX_AUTO_HOP_EN	TX AUTO HOP enabling 0：disable 1：enable
	2	RW	TX_ACK_EN	Enabling ACK function under TX mode 0：disable 1：enable
	1	RW	TX_DC_PERSIST_EN	Configuration of duty cycle transmission in TX mode. 0: exit when the number of times configured in TX_DC_TIMES is reached. 1: keep in duty cycle mode until this bit is configured as 0.
	0	RW	TX_DC_EN	TX Duty Cycle enabling 0: disable 1: enable
CTL_REG_97 (0x61)	7	RW	CSMA_EN	CSMA enabling 0: disable 1: enable
	6:4	RW	RX_EXIT_STATE<2:0>	Exiting the setting status automatically once it completed the receiving. 1：SLEEP 2：READY 3：TFS

Register Name	Bits	R/W	Bit Flag	Description
				4：TX 5：RFS 6：RX Others：SLEEP The chip only exits RX automatically after receiving completes under packet mode, otherwise it will wait until the MCU sends the go_* command to switch.
	3	RW	RX_TIMER_EN	RX TIMER enabling 0: disable 1: enable
	2	RW	RX_ACK_EN	RX ACK enabling 0: disable 1: enable
	1	RW	RX_AUTO_HOP_EN	RX AUTO HOP enabling 0: disable 1: enable
	0	RW	RX_DC_EN	RX Duty Cycle enabling 0: disable 1: enable
CTL_REG_98 (0x62)	7	RW	PKT_DONE_EXIT_EN	Whether stays in the current state or immediately returns back to the RX_EXIT_STATE configured state after receiving the PKT_DONE signal. 0: stay in current state after receiving the PKT_DONE signal. 1: return to the state configured in RX_EXIT_STATE.
	6:4	RW	RX_HOP_SLP_MODE<2:0>	There are 7 modes to select in low power auto-frequency-hopping configuration. More details please refer to table 4.
	3:0	RW	SLP_MODE<3:0>	There are 14 modes to select in selection of low power receiving configuration. More details please refer to table 5.
CTL_REG_99 (0x63)	7:0	RW	SLEEP_TIMER_M<7:0>	The counting time of SLEEP TIMER is defined as the formula of: T = M x 2^(R+1) x 31.25 us The values of R range from 0-26
CTL_REG_100 (0x64)	7:5	RW	SLEEP_TIMER_M<10:8>	
	4:0	RW	SLEEP_TIMER_R<4:0>	
CTL_REG_101 (0x65)	7:0	RW	RX_TIMER_T1_M<7:0>	The counting time of RX T1 TIMER is defined as the formula of: T = M x 2^(R+1) x 20 us The values of R range from 0-21
CTL_REG_102 (0x66)	7:5	RW	RX_TIMER_T1_M<10:8>	
	4:0	RW	RX_TIMER_T1_R<4:0>	
CTL_REG_103 (0x67)	7:0	RW	RX_TIMER_T2_M<7:0>	The counting time of RX T2 TIMER is defined as the formula of: T = M x 2^(R+1) x 20 us
CTL_REG_104	7:5	RW	RX_TIMER_T2_M<10:8>	

Register Name	Bits	R/W	Bit Flag	Description
(0x68)	4:0	RW	RX_TIMER_T2_R<4:0>	The values of R range from 0-21
CTL_REG_105 (0x69)	7:6	RW	RESV	Reserve bit can only be set as 0.
	5:4	RW	TIMER_RAND_MODE<1:0>	The random mode of CSMA SLEEP TIMER configured under CSMA: 00：Random R value 01：Random M value 10：Both of the R value and M are random 11：Use the configured fixed value
	3	RW	SLEEP_TIMER_EN	SLEEP TIMER enabling： 0：disable 1：enable
	2	RW	RESV	Reserve bit and it only can be writen as 0
	1	RW	LFCLK_SEL	Selection of low frequency clock source： 0：LFOSC 1：LFXO
	0	RW	LFCLK_OUT_EN	The enabling of output low-frequency clock to GPIO4. 0: disable. 1: enable. The priority of this item is lower than DIG_CLKOUT_EN and higher than GPIO4_SEL.
CTL_REG_106 (0x6A)	7:5	RW	CSMA_CCA_MODE<2:0>	The condition used to judge that a signal channel is busy in CSMA mode. 000: always recognize the signal channel as busy. 001: RSSI detected valid no less than once within 4 detection windows. 010: PJD detected valid no less than once within 4 detection windows. 011: RSSI or PJD detected valid no less than once within 4 detection windows. 100: detect SYNC_PASS once. 101: detect SYNC_PASS once or detect RSSI valid no less than once within 4 detection windows. 110: detect SYNC_PASS once or detect PJD valid no less than once within 4 detection windows. 111: detect SYNC_PASS once or detect RSSI or PJD valid no less than once within 4 detection windows.
	4	RW	CSMA_PERSIST_EN	CSMA operating selection： 0: exit CSMA mode if the signal channel is still busy when the number of maximum detection times is reached. 1: keep on detecting signal channel state until it becomes idle and then transmits the data out.

Register Name	Bits	R/W	Bit Flag	Description
	3:2	RW	CSMA_CCA_INT_SEL<1:0>	CSMA_CCA_INT interrupt condition： 00：PJD is valid 01：RSSI is valid 10：Both of PJD and RSSI are valid 11：NA
	1:0	RW	CSMA_CCA_WIN_SEL<1:0>	The size of a single detection window in CSMA： 00：32-symbol 01：64-symbol 10：128-symbol 11：256-symbol
CTL_REG_107 (0x6B)	7:0	RW	RX_TIMER_CSMA_M<7:0>	The counting time of RX CSMA TIMER is defined as the formula of: T = M x 2^(R+1) x 20 us The value range of R is 0 - 21.
CTL_REG_108 (0x6C)	7:5	RW	RX_TIMER_CSMA_M<10:8>	
	4:0	RW	RX_TIMER_CSMA_R<4:0>	
CTL_REG_109 (0x6D)	7:0	RW	LBD_TH<7:0>	If the value is under the low voltage detection threshold, it is recognized as low voltage state.
CTL_REG_110 (0x6E)	7:0	RW	TX_DC_TIMES<7:0>	Setting the maximum transmitting number in non-Persistent under TX Duty Cycle mode.
CTL_REG_111 (0x6F)	7	RW	LENGTH_MODE	Length filed structure selection 0: cmt2200 normal packet structure，Value of the Length field equals to packet length. 1: As the Wi-sun packet structure shown in Figure 1, the higher 5 bit of the Length filed is CTL_REG_111[4:0] and the lower 11 bit is the length of PSDU field.
	6	RW	WISUN_ALLIN	Configuration source of FCS field and DW field 0: Both of the FCS field and DW field are decided by system configuration, while WISUN_FCS and WISUN_DW are invalid. 1: Both of the FCS field and DW field are decided by WISUN_FCS and WISUN_DW, which are compatible with Wi-sun protocol.
	5	RW	WHITEN_WISUN	Whitening polynomial selection 0：cmt2200 normal packet supports for 3 kinds of whitening polynomial. 1：Wi-sun protocol supports for whitening polynomial.
	4	RW	WISUN_MS	Default as 0
	3:2	RW	RESV	Reserve bit and it has to write as 0
	1	RW	WISUN_FCS	CRC bytes of PSDU field 0: 4 Bytes 1: 2 Bytes
	0	RW	WISUN_DW	Whitening enabling of PSDU field

Register Name	Bits	R/W	Bit Flag	Description
				0：disabling 1：enabling
CTL_REG_112 (0x70)	7:0	R	TX_DC_DONE_TIMES<7:0>	Transmission times completed under TX Duty Cycle mode.
CTL_REG_113 (0x71)	7:0	RW	TX_RS_TIMES<7:0>	The specified maximum number of repeat transmission under TX ACK mode.
CTL_REG_114 (0x72)	7:0	R	TX_RS_DONE_TIMES<7:0>	The already repeat transmission times under TX ACK mode.
CTL_REG_115 (0x73)	7:0	RW	CSMA_TIMES<7:0>	The maximum detection times in the non-persistent mode under CSMA.
CTL_REG_116 (0x74)	7:0	RW	CSMA_DONE_TIMES<7:0>	The already repeat transmission times under CSMA mode.
CTL_REG_118 (0x76)	7:0	RW	SLEEP_TIMER_CSMA_M<7:0>	The counting time of SLEEP CSMA TIMER is defined as the formula of： T = M x 2^(R+1) x 31.25 us The value of Ranges from 0 to 26.
CTL_REG_119 (0x77)	7:5	RW	SLEEP_TIMER_CSMA_M<10:8>	
	4:0	RW	SLEEP_TIMER_CSMA_R<4:0>	
FIFO_PORT (0x7A)	7:0	W	FIFO_RW_PORT<7:0>	It is not a register but a port for FIFO read and write operation. More information please refer to the serial port operation description.
CRW_PORT (0x7B)	7:0	W	REG_CRW_PORT<7:0>	It is not a register but a port for register batch reading and writing operation. More information please refer to the serial port operation description.
PAGE_CTL (0x7E)	7:6	RW	PAGE_SEL<1:0>	It is used for select the page 0, 1, 2 of register： 00：PAGE 0 01：PAGE 1 10：PAGE 2 11：NA，not allowed to write Regardless of whether the current page is 0,1, or 2, pages can be switches by setting the PAGE_CTL register of 0x7A, which can reflect the current page of the bit.
	5:0	RW	RESV	Reserve bit and it has to write as 0.
SOFT_RST (0x7F)	7:0	W	SOFTRST	Soft reset address.

Table 1. Low-power Receiving Options Defined in RX_HOP_SLP_MODE<2:0>

No.	Extension way of RX	Condition for RX Extension
0	If it is configured as 0, there's no extension and it will exit RX when T1 counting ends.	None
1	Once the chip meets detection conditions within T1, it will exit T1 and hand over control to MCU.	RSSI_VLD is valid
2		PREAM_OK is valid
3		Both of the RSSI_VLD and PREAM_OK are valid.
4	Once T1 meets the detection conditions, it will switch to T2; and then once it detects SYNC, it will exit T2 and hands over control to MCU, otherwise it exits RX when T2 ends.	RSSI_VLD is valid
5		PREAM_OK is valid
6		Both of the RSSI_VLD and PREAM_OK are valid.

Table 5. 14 Low-power Receiving Options Defined in SLP_MODE<2:0>

No.	Extension way of RX	Condition for RX Extension
0	RX If it is configured as 0, there's no extension and it will exit RX when T1 counting ends.	None
1	Once it meets detection conditions within T1, the chip exits T1 and hands over control to MCU.	RSSI_VLD is valid
2		PREAM_OK is valid.
3		Both of the RSSI_VLD and PREAM_OK are valid.
4	Once it detects RSSI valid within T1, the chip exits T1 and stays in RX until RSSI unsatisfied and then it exits RX.	RSSI_VLD is valid.
5	Once it meets detection conditions within T1, the chip switches to T2; and then it exits RX when T2 ends.	RSSI_VLD is valid.
6		PREAM_OK is valid.
7		Both of the RSSI_VLD and PREAM_OK are valid.
8		Either PREAM OK or SYNC OK is valid
9		Either PREAM_OK or NODE_OK is valid
10		Either PREAM OK, SYNC OK, or NODE OK is valid
11	Once T1 meets the detection conditions, it will switch to T2; and then once it detects SYNC, it will exit T2 and hands over control to MCU, otherwise it exits RX when T2 ends	RSSI_VLD is valid.
12		PREAM_OK is valid.
13		Both of the RSSI_VLD and PREAM_OK are valid.

1.3 PAGE 1, Configuration Register（0x00 - 0x68）

Table 4. Control Register in PAGE 1 (0x00 - 0x68)

Register Name	Bits	R/W	Bit Name	Description
CMT configuration area (0x00 - 0x0F)	7:0	RW	Inaccessible	Dedicated registers for CMT usage. The register content is exported from RFPDK and register values are depend on factory test.
TX configuration area (0x10 - 0x27)				Configuration registers for TX parameters. The register content output through RFPDK, which is generated from user configurations.
RX configuration area (0x30 - 0x61)				Configuration registers for RX parameters. The register content output through RFPDK, which is generated from user configurations.
RX_RSSI_REG_00 (0x62)	7:6	RW	RESV	Reserve bit and it has to write as 0.
	5:4	RW	COLL_STEP_SEL<1:0>	Threshold for anti-collision detection：00: 6dB

Register Name	Bits	R/W	Bit Name	Description
				01: 10dB 00: 16dB 00: 20dB
	3:2	RW	RSSI_UPDATE_SEL	Update condition of RSSI value (with unit of dbm) : 00：Keep update at current time 01：Update after receiving PREAM_OK 10：Update after receiving SYNC_OK 11：Update after receiving PKT_DONE
	1	RW	RESV	Reserve bit and it has to write as 0.
	0	RW	COLL_DET_EN	Anti-signal collision detection enabling： 0：disable 1：enable
RX_RSSI_REG_01 (0x63)	7:0	RW	RSSI_ABS_TH<7:0>	Threshold for valid RSSI with unit of dbm.
RX_DOUT_REG_00 (0x64)	4:2	RW	DOUT_ADJUST_SEL<2:0>	The adjusted percentage of duty cycle： 0：3.33% 1：6.66% 2：9.99% 3：13.32% 4：16.65% 5：19.98% 6：23.21% 7：26.64%
	1	RW	DOUT_ADJUST_MODE	The adjusted direction of duty cycle. 0: increase duty cycle by 1. 1: decrease duty cycle by 1.
	0	RW	DOUT_ADJUST_EN	The enabling adjusted percentage of duty-cycle output: 0：disable 1：enable
RX_ANTD_REG_00 (0x67)	3:2	RW	ANT_WAIT_PMB<1:0>	The waiting Preamble length of antenna calibration: 00: RX_PREAM_SIZE x 1.5 01: RX_PREAM_SIZE x 2 10: RX_PREAM_SIZE x 2.5 11: RX_PREAM_SIZE x 3
	1	RW	ANT_SW_DIS	Enable the antenna skipping switch: 0：enable antenna switch 1：disable antenna switch
	0	RW	ANT_DIV_EN	The antenna diversity enabling: 0：disable 1：enable

2 Revise History

Table 5. Revise History Record

Version No.	Chapter	Description	Date
0.5	All	The initial version	2020-09-17
0.6A	All	Review	2022-01-09
0.7	All	Review	2022-08-12

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