CMOSTEK

AN238

CMT2310A RF Parameter Configuration Guide

Overview

This document discusses the RF, OOK/FSK demodulation related parameter configuration on RFPDK tool.

The part number covered by this document is shown as below.

Table 1. Part Numbers Covered in this Document

Part Number	Frequency	Modem	Function	Configuration	Package
CMT2310A	117 - 1050MHz	(4)(G)FSK/OOK	Transceiver	Register	QFN24

Before reading this document, users can read *AN237 CMT2310A Quick Start Guide* first to get basic using information of CMT2310A.

Table of Contents

1. Tx and Rx Parameter Configuration

1.1 Basic Parameter Configuration

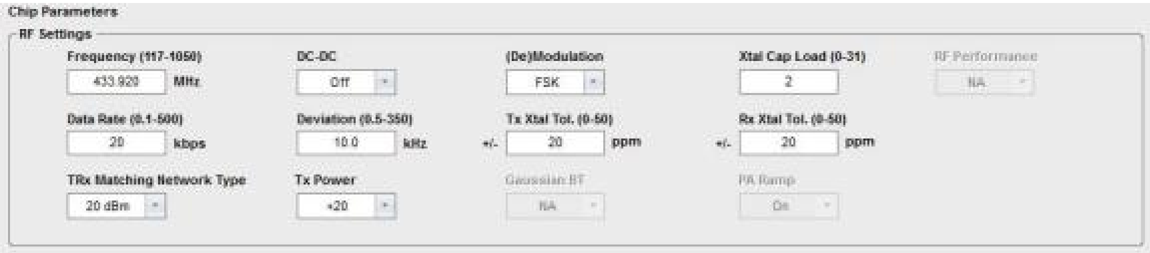

Figure 1. Tx and Rx Parameter Configuration GUI

The registers corresponding to above parameters are stored in frequency area, data rate area and transmission area, all of which comes from complicated calculation and users don't need to understand the process. Although the RFPDK GUI parameters are easily understandable there still has some configurations need to be specially focused.

- **How to select Deviation**

For 2(G)FSK, *Deviation* refers to distance from frequency point of *0* or *1* to central frequency point.

For 4(G)FSK, *Deviation* refers to the distance from the frequency point at the far end to the central frequency point.

Table 2. Deviation Selection

	Only use TX $F_{dev_TX_only_}$max	Only use RX $F_{dev_RX_only_}$max	TRX $F_{dev_TRX_}$max	Unit
675 - 960 MHz	600	350	350	kHz
450 - 640 MHz	400	350	350	kHz
338 - 450 MHz	300	350	300	kHz
225 - 320 MHz	200	350	200	kHz
169 - 225 MHz	150	350	150	kHz
135 - 169 MHz	120	350	120	kHz
113 - 135 MHz	100	350	100	kHz

The corresponding F_{dev}_max is chosen by the operating frequency and practical application. RFPDK is defaulted to use TRX.

If both TX and RX deviation need to be configured separately, please bring up the detailed requirements.

For 2(G)FSK, it is suggested to meet the following requirements to configure Deviation:

1. Deviation < F_{dev}_max, and Data Rate * 0.50 + Deviation<= F_{dev}_max;
2. Data Rate * 0.25 <= Deviation, that is, the modulation index must not less than 0.5 (MSK);

3.If Data Rate * 0.5 <= Deviation <= Data Rate * 2 under the cases of both 1 and 2, it means it can achieve the optimum sensitivity.

For 4(G)FSK, it is suggested to meet the following requirements to configure Deviation:

1. Deviation < F_{dev}_max and Data Rate * 0.25 + Deviation<= F_{dev}_max;

2. Data Rate * 0.125 <= Deviation;

3. If Data Rate * 0.25<= Deviation <= Data Rate * 2 under the cases of both 1 and 2, it means it can achieve the optimum sensitivity.

- **How to select the crystal PPM**

Users are required to input crystal tolerances for Tx and Rx on RFPDK GUI respectively. Supposing input +/-20 ppm respectively, it means that crystal frequency deviation is 40 ppm between the transmitter and receiver in the worst case. Users need to set the two tolerance parameters by considering the worst case, which affect each bandwidth settings in the receiver.

- **How to select TRX matching network type**

The matching network type is selected according to the highest power (13 dBm or 20 dBm), which helps to improve the PA efficiency and reduce emission current.

1.2 OOK Demodulation Configuration

Figure 2. OOK Configuration GUI

Suggestions for OOK demodulation configuration are shown as follow.

Table 3. OOK Parameter Configuration Suggestion

RFPDK Input Parameter	Configuration Suggestion
Demod Method	For *Middle*, the demodulation responding is fast. The advantage is that it can correctly demodulate immediately every time after a communication starts. The disadvantage is that if there is a spike
	mutation in the packet (a sudden abrupt increase in amplitude), it will affect the demodulation in the subsequent period. For *Average*, the demodulation responding is slow. The disadvantage is that it takes some time to start demodulate correctly (usually 10 - 20 symbols) for each communication. The advantage is that the demodulation will not be affected if there is a spike mutation in the packet. In practice, the spike mutation only exists in some special applications such as the case of poor performance of AC to DC power supply to the chip. Therefore, apart from the special cases, it is generally recommended that the demodulation method *Middle* is selected to speed up demodulation and reduce receiving time.
Long-Zero Number	Users need to input this value to tell the receiver how many consecutive *0* possibly exist at most in a packet. Then the receiver will tune the relevant parameters to ensure the best demodulation result.

1.3 FSK Demodulation Configuration

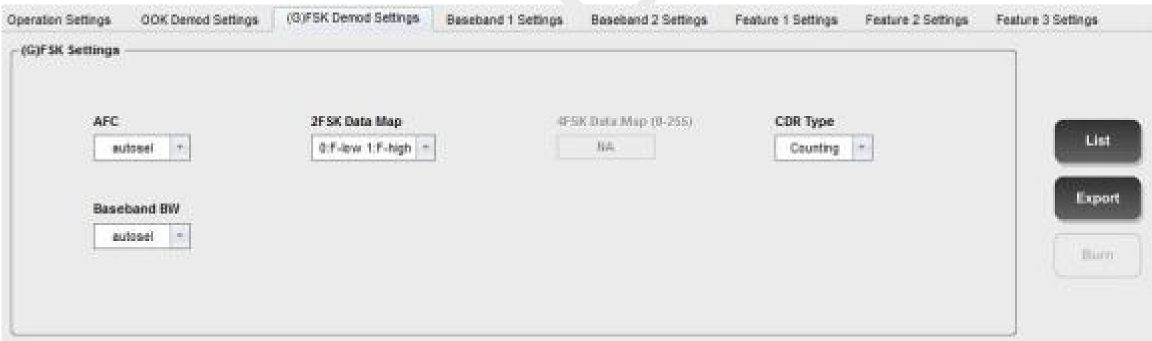

Figure 3. FSK Demodulation Configuration GUI

Table 4. FSK Parameter Configuration Suggestion

RFPDK Input Parameter	Configuration Suggestion
AFC	AFC switch is recommended to be opened on general.
CDR Type	In the packet mode, as it needs to detect Preamble or Sync, the symbol rate clock recovery function should be enabled. More information for CDR usage will introduce in the following chapter.
CDR DR Range	The maximum deviation range of the symbol length can be traced by CDR under Tracing mode.
2FSK Data Map	Select the two frequency points of 2FSK, which stands for 0 and stands for 1. Usually, the default value is selected.

4FSK TX Data Map	TX terminal Bits [7:6] stand for the value representing the highest frequency point; Bits [5:4] stand for the value representing the second highest frequency point; Bits [3:2] stand for the value representing the second lowest frequency point; Bits [1:0] stand for the value representing the lowest frequency point.
4FSK RX Data Map	RX terminal Bits [7:6] stand for the value representing the highest frequency point; Bits [5:4] stand for the value representing the second highest frequency point; Bits [3:2] stand for the value representing the second lowest frequency point; Bits [1:0] stand for the value representing the lowest frequency point.

1.4 CDR Parameters and CDR Mode

The corresponding RFPDK GUI and parameters are shown as follow.

Figure 4. CDR Configuration Parameter

The suggestions on CDR demodulation configuration are as follow.

Table 5. CDR Parameter Configuration Suggestion

RFPDK Parameter	Register Bits
CDR Type	CDR_MODE< 1:0>
CDR DR Range	CDR_RANGE_SEL< 1:0>
It is automatically selected by RFPDK according to related parameters and no need for users to select.	CDR_DET_SEL
It is automatically selected by RFPDK according to related parameters and no need for users to select.	CDR_AVG_SEL<2:0>
It is automatically selected by RFPDK according to related parameters and no need for users to select.	CDR_3RD_EN
It is automatically selected by RFPDK according to related parameters and no need for users to select.	CDR_4TH_EN
It is automatically selected by RFPDK according to related parameters and no need for users to select.	CDR_BR_TH< 15:8>

The related registers information is shown as below.

Table 6. CDR Related Register Description

Register Name	Bit	R/W	Bit Name	Function Description
RX_CDR_REG_00 (Page1, 0x44)	7	RW	CDR_DET_SEL	In tracing mode, select the way of data rate detectio： 0： way 0 1： way 1 Way 1 is selected by default, users don't need to understand the bit.
	6:4	RW	CDR_AVG_SEL<2:0>	In tracing mode, the average filter order of the CDR output： 0： 6/8 1： 1/2 2： 6/ 16 3： 1/4 4： 11/64 5： 1/8 6： 3/32 7： 1/ 16
	3:2	RW	CDR_RANGE_SEL< 1:0>	In tracing mode, the maximum deviation range of the symbol length can be traced by CDR: 0: +/-6.3% (Symbol rate range is from -5.9% to +6.7%) 1: +/-9.4% (Symbol rate range is from -8.6% to + 10.4%) 2: +/- 12.5% (Symbol rate range is from - 11. 1% to + 14.3%) 3: +/- 15.6% (Symbol rate range is from - 13.5% to + 18 5%)
	1:0	RW	CDR_MODE< 1:0>	CDR mode selection： 0： tracing 1： counting 2： Manchester 3： no cdr More information will describe at the following chapter.
RX_CDR_REG_03 (Page1, 0x47)	4	RW	CDR_4TH_EN	In tracing mode, enable data rate detection when there is no flip for 4 consecutive symbols: 0： disable 1： enable
	3	RW	CDR_3RD_EN	In tracing mode, enable data rate detection when there is no flip for 3 consecutive symbols: 0： disable 1： enable
	2:0	RW	CDR BR TH< 18: 16>	Same as the follow
RX_CDR_REG_01 (Page1, 0x45)	7:0	RW	CDR_BR_TH<7:0>	In tracing mode, the threshold needed by CDR

RX_CDR_REG_02 (Page1, 0x46)	7:0	RW	CDR_BR_TH< 15:8>	can be calculated as: TH = crystal frequency/ data rate. For example, when the data rate is 15 kHz and the crystal frequency is 32 Mhz, the result can be rounded to 2133

The CMT2310A 's clock recovery related parameters are stored in the data rate bank, automatically configured by RFPDK. Users do not need to understand the register content if no other special requirements. The following chapter will introduce the design specifications and mode selection of clock recovery. Clock recovery is referred to as CDR.

The basic task of a CDR system is to recover the clock signal that is synchronized with the data rate while receiving data, which can not used for decoding chip internerly, but also output to GPIO for users to sample the data. Therefore, CDR's task is simple

but important. If there's a deviation between the recovered clock frequency and the actual data rate, it will cause data collection error, error code and decoding error while receiving.

In fact, the application environment will be not that ideal as expected, so there will be 2 situations when the system works.

1. The data rate of TX and RX configuration is well aligned, or the deviation is as small as 1/ 10,000th or 1/thousandth, which is usually for the reason that TX and RX configuration and data rate calculation mechanism are relatively advanced, such as various high-end TRX products are used.

2. The data rates of TX and RX configurations vary greatly, that is, from a few hundredths to several tenths.

At the same time, there are 3 important indicators:

1. The length of data that can be correctly sampled in case of no data flipping (keep receiving consecutive 0 or 1).
2. The maximum bearable data rate deviation between TX and RX.
3. Make sure if the sensitivity can be improved and error can be reduced.

There are 3 sets of CDR system inside CMT2310A according to the 2 application situations and the 3 indicators. They will be shown in the following content.

- **COUNTING System**

If the symbol rate is 100% aligned, the unlimited 0 length can be received continuously without error. However, if a deviation exists, the deviation will be accumulated in case of receiving non-flipping data. For example, if the symbol deviation is 5%, then for 10 consecutive symbols without flipping, the deviation will be accumulated to over 50%, possibly causing a sampling error, which is similar to the traditional UART transmission. Once the signal is flipped, the deviation will be cleared and a new accumulation begins. Therefor, if the deviation is very small, for example, it is 1/5000, users can continuously receive 2500 non-flipping symbols with no error, which can be considered a good performance.

- **TRACING System**

The system is designed for relatively large symbol rate deviation and has tracing function. It can automatically detect the symbol rate transmitted by TX, and quickly adjust the local symbol rate of RX meanwhile, so as to minimize the deviation between them. The system can withstand a deviation up to 15.6%, which is quite a remarkable performance among similar products in the industry. On the other hand, the system functioning depends on the accuracy of the local symbol rate adjustment. Since the crystal frequency is fixed at 32 MHz, the higher the symbol rate, the lower the accuracy of the adjustment. Generally speaking, the accuracy will be higher if the symbol rate is under 50 kHz. It can receive more continuous non-flipping data without error. That is, the lower the symbol rate is, the more correct data is sampled. The actual number of sampled symbols is obtained by measurement. If the symbol rate is above 50 kHz, the amount of non-flipping data that can be sampled correctly will become less and less. If the symbol rate is up to 250 kHz, possibly only 2-3 bytes of non-flipping data can be sampled correctly.

Note：4FSK/4GFSK only support for Counting mode.

- **MANCHESTER System**

This system is derived from the COUNTER system, and they share the basic same characteristics. The only difference is that the system is designed specifically to Manchester codec, providing special processing upon unexpected change in TX symbol rate. A kind of unexpected change happens frequently is that: sometimes TX data contains 2 consecutive 0 or 1 after Manchester encoding; If one of the length of symbol *0* or *1* suddenly becomes longer than 50%, the RX may sample them as three *0* or *1*; If the symbol length suddenly becomes shorter over 50%, RX may only sample then as one *0* or *1*; to handle such special cases, in CDR system, the sampling will stop if 3 or more non-flipping symbols are detected in the received data ,to prevent error occurred from the sudden longer of the symbol;on the other hand, if the symbol becomes shorter, users can speed up the RX symbol rate to ensure sampling correctly even when the symbol length is shorter over 50%.

How to select the suitable CDR system

RFPDK will select the CDR system automatically according to the configuration of the symbol rate. When the symbol rate is no more than 50 kHz, the TRACING system is selected, which can not only realize tracing function but also sample correctly with long non-flipping data. When the symbol rate is more than 50 kHz and less than 200 kHz, it can be set according to user requirements. If users tend to accept the more symbol rate error, TRACING system can be selected; if users prefer to achieve longer non-flipping data, COUNTING system can be chosen. When the symbol rate is more than 200 kHz, TRACING performs better than COUNTING. When the entire packet conforms to the Manchester coding rule (i.e., no more than 2 consecutive non-flipping symbols), and unexpected change in symbol rate exists in the application, MANCHESTER system can be considered.

In addition, no matter which type of CDR system is selected, when CDR is enabled it can improve the sensitivity by 1-2 dB in comparison with receiving RAW data.

- **How to debug the TRACING parameter:**

In tracing system, the tracing function is conducted upon each data flipping. The ideal situation is that it adjusts each symbol when the packet contains preamble so as to achieve the fastest tracing.

The debugging methods of a few parameters are provided below.

CDR_RANGE_SEL<1:0>

This parameter is to select the symbol rate deviation that can be tracing. The percentage given in the register is not the percentage of symbol rate but the percentage of symbol length. For example, if the symbol rate is 10 kHz, a symbol length is 100 ns; then +/- 15.6% means that, if the TX symbol length is in the range of 84.4 ~ 115.6 ns, then RX can detect the symbol length and adjust its local length to TX side, so as to eliminate the symbol rate deviation. In conversion from percentage of symbol length to that of symbol rate, a length percentage + 15.6% can be converted to a symbol rate percentage of - 13.5%, and same way - 15.6% can be converted to + 18.5%.

Users might doubt that why not select the maximum tracing range. The larger the tracing range is, the more difficult it is to trace and the longer it may take. Therefore, users are advised to select the most appropriate range based on actual application requirements

- **CDR_3RD_EN，CDR_4TH_EN**

These two parameters are associated with CDR_RANGE_SEL< 1:0>. When +/- 15.6% is selected, none of them can be enabled. When +/- 12.5% is selected, CDR_4TH_EN disabled. Apart from the above 2 cases, others are enabled. The details will not be discussed here.

- **CDR_AVG_SEL<2:0>**

The smaller the filter coefficient, the narrower the bandwidth, the slower the tracing symbol rate, the smoother the output. The larger the filter coefficient is, the wider the bandwidth; the faster the tracing symbol rate and the more jitter when it outputs. This is similar to how PLL works. Usually we hope that the tracing can be as fast as possible (for example, completes within several symbols in front of preamble), and output stably; otherwise it is easy to cause code error afterwards, especially where there are more long continuous 0 or 1 in a packet. Therefore, if users want to adjust this parameter by themselves, it is necessary to debug and observe the effect according to the actual situation.

Besides, generally the higher the symbol rate is, the more jitter it will be. Therefore, users should consider to set smaller filter coefficient to improve the receiving accuracy of data containing long continuous 0 or 1. However users need to have a trade-off of the acceptance of slow tracing.

1.5 Register Classification and Usage in the Tx Bank

Usually, register content in Tx bank is entirely generated by the RFPDK and users only need to configure registers once in chip initialization stage. Considering that users might modify the parameters such as Tx power, symbol rate individually during application process, the Tx bank can be further categorized, which is convenient for targeted configuration by users.

Table 7. TX Bank Registers Category

Address	Port Bus	Default	Name	Description
0x10	RW	0x00	**TX_FREQ_REG_00**	TX Freq
0x11	RW	0x00	**TX_FREQ_REG_01**	
0x12	RW	0x00	**TX_FREQ_REG_02**	
0x13	RW	0x00	**TX_FREQ_REG_03**	
0x14	RW	0x00	**TX_MODE_REG_00**	TX Mode
0x15	RW	0x00	**TX_DR_REG_00**	TX Data Rate
0x16	RW	0x00	**TX_DR_REG_01**	
0x17	RW	0x40	**TX_DR_REG_02**	
0x18	RW	0x80	**TX_DR_REG_03**	
0x19	RW	0x60	**TX_DR_REG_04**	
0x1A	RW	0x08	**TX_DR_REG_05**	
0x1B	RW	0x00	**TX_DEV_REG_00**	TX Dev
0x1C	RW	0x00	**TX_DEV_REG_01**	
0x1D	RW	0x00	**TX_DEV_REG_02**	
0x1E	RW	0x00	**TX_PWR_REG_00**	TX Power
0x1F	RW	0x40	**TX_PWR_REG_01**	
0x20	RW	0x00	**TX_PWR_REG_02**	

0x21	RW	0x00	**TX_PWR_REG_03**	
0x22	RW	0x00	**TX_PWR_REG_04**	
0x23	RW	0x00	**TX_PWR_REG_05**	
0x24	RW	0x00	**TX_PWR_REG_06**	
0x25	RW	0x00	**TX_MISC_REG_00**	TX Misc
0x26	RW	0x00	**TX_MISC_REG_01**	
0x27	RW	0x00	**TX_MISC_REG_02**	

Table 8. TX Bank Registers Category

Category	Description
TX Freq	Tx frequency settings.
TX Mode	Tx mode settings.
TX Data Rate	Tx data rate and Ramp control settings.
TX Dev	Tx Deviation settings.
TX Power	Tx power settings.
TX Misc	Other settings.

Although users do not need to understand the content of theses registers, Users can target the configuration and try to reduce the register input number.

2. Revise History

Table 9. Revise History Record

Version No.	Chapter	Description	Date
0.5	All	Initial version	2020-09-17
0.6A	All	Review	2022-01-09
0.6C	All	Review	2022-08-04
0.7	All	Review	2022-08-18

3. Contacts

CMOSTEK Microelectronics Co., Ltd. Shenzhen Branch

Address: 30th floor, 8th Building, C Zone, Vanke Cloud City, Xili Sub-district, Nanshan, Shenzhen, GD, P.R. China

Post code： 518055

Tel： +86-755-83231427
Sales： sales@cmostek.com

Supports： support@cmostek.com

Website： www.cmostek.com